

State-of-the-art in-situ metrology during OMVPE in academic research and industry

Kolja Haberland
LayTec AG, Berlin, Germany

Acknowledgements



Martin Zorn

JENOPTIK Diode Lab GmbH, Berlin, Germany



Arne Knauer, Frank Brunner, Andre Maaßdorf,
Markus Weyers

Ferdinand-Braun-Institut, Berlin, Germany



Benjamin Buick, Claudine Groß, Christian Kaspari,
Thomas Wand, Johannes K. Zettler, Thomas Zettler
LayTec AG, Berlin, Germany

Outline

In-situ metrology for MOCVD – a brief sketch of historical development

Current metrology challenges

State-of-the-art metrology for VCSEL/DBR/SESAM

UV-LEDs: in-situ metrology for high Al-containing III-Ns

Summary and outlook

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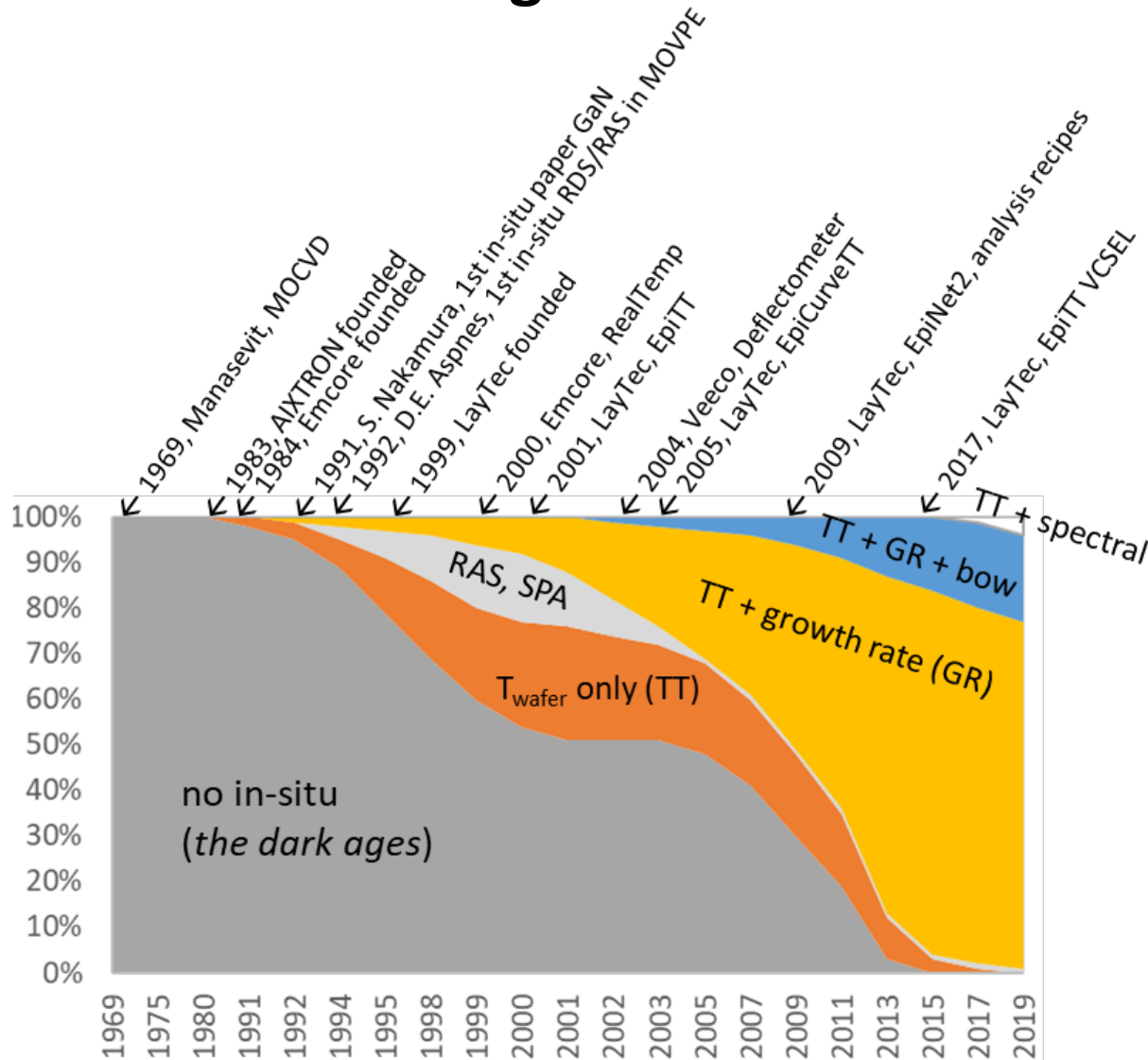
Summary and outlook

In-situ monitoring for MOCVD – historical development



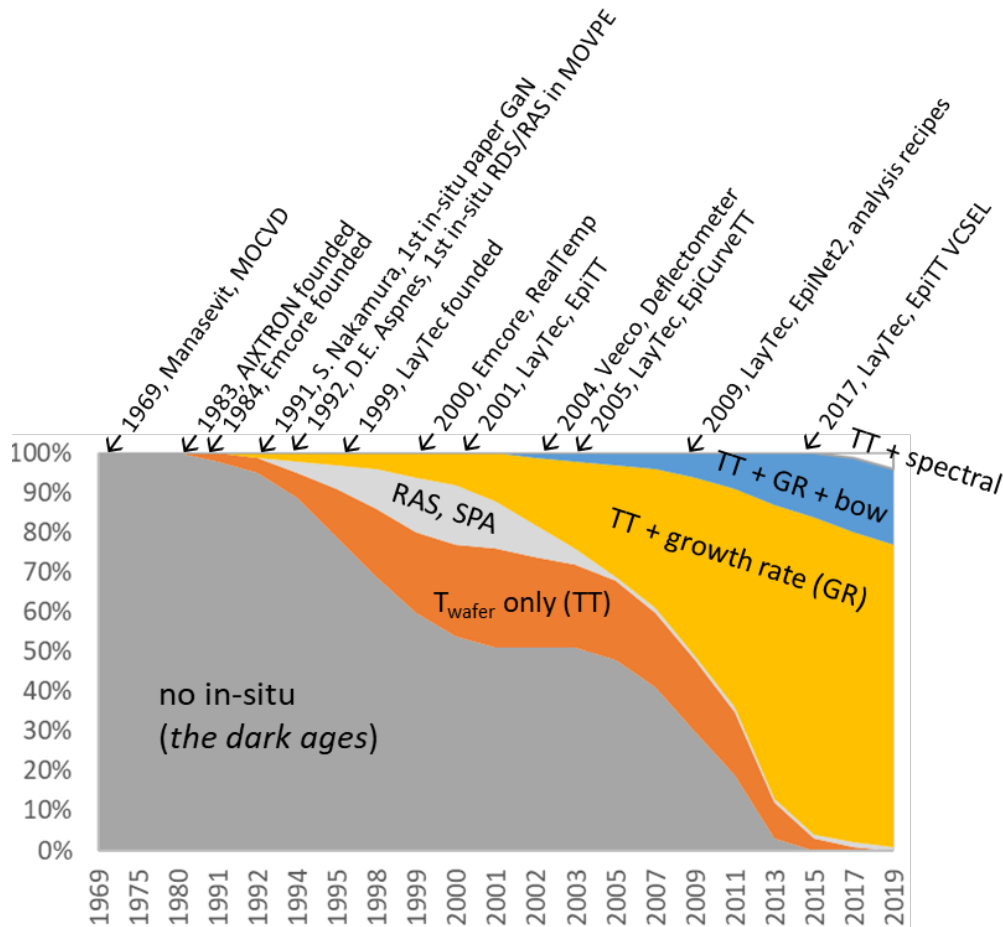
Carl Spitzweg: "Der Alchimist" (1860)

In-situ monitoring for MOCVD – historical development



RAS = reflectance anisotropy spectroscopy
 SPA = surface photo absorption
 TT = true temperature measurement
 GR = growth rate measurement
 bow = wafer bow/curvature measurement

In-situ monitoring for MOCVD – historical development



*Ben Stevens et al. (IQE),
CSManTech, May 2019:*

“All VCSEL reactors at IQE use a LayTec EpiTT ... The LayTec system also enables characterization of critical layers in a VCSEL that could not be characterized by traditional means or would require complicated modelling. Through use of analysis recipes the required analysis can be loaded into the MES before the wafers are even unloaded from the reactor.”

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In-situ metrology for MOCVD – a brief sketch of historical development

Current metrology challenges

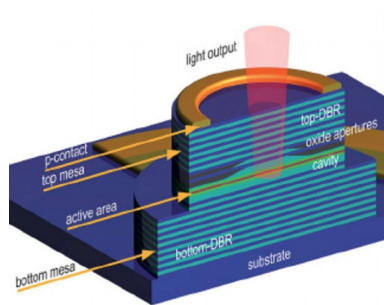
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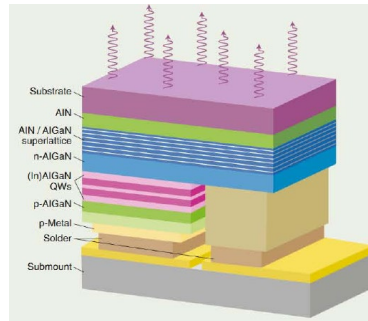
Current metrology challenges

VCSEL on GaAs



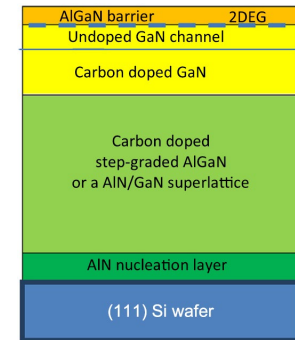
- >100 layers; >5 μm stack
- 0.1% accuracy in growth rate
- pyrometry blocked by DBR
- x_{AlGaAs} for oxide aperture
- **graded interfaces** in DBRs
- nm-scaled layers (MQW, grading)

UV-C LED on sapphire



- 2-step epi (AlN/sapph + LED)
- >3 μm stack
- all layers $k=0$
- no access to T_{wafer}
- **surface roughness** ($x_{\text{AlGaIn}} > 0,5$)
- High strain (AlGaIn on AlN)
- nm-scaled layers (MQW, SL, EBL)

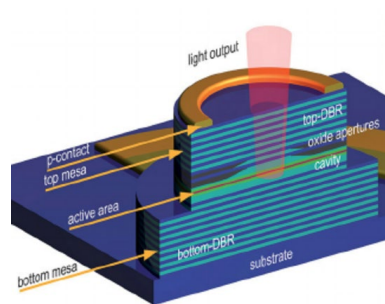
GaN Power HEMT on Si



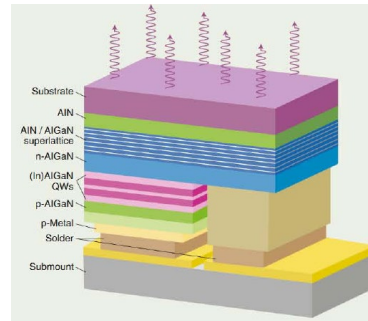
- Large wafers + large bow
- Pyrometry: GaN is ARC on Si, 40% oscillations in emissivity
- >3 μm stack, all layers $k=0$
- **Wafer temperature during AlGaIn barrier growth** extremely critical

Current metrology challenges

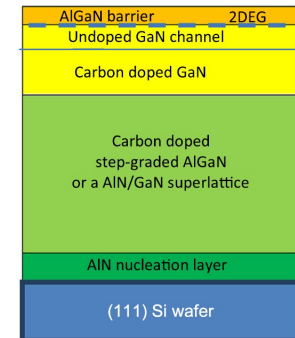
VCSEL on GaAs



UV-C LED on sapphire



GaN Power HEMT on Si

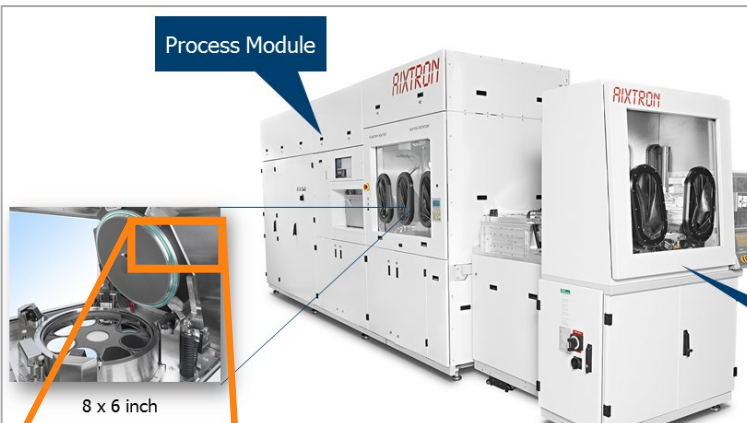


These three very different device structures have in common:

- >5 hours of Epi
- wafer temperature measurement is very difficult
- high-yield manufacturing is not possible without in-situ metrology

Market leading MOCVD tool for VCSELs, GaN/Si HEMTs: AIXTRON planetary G4/G5

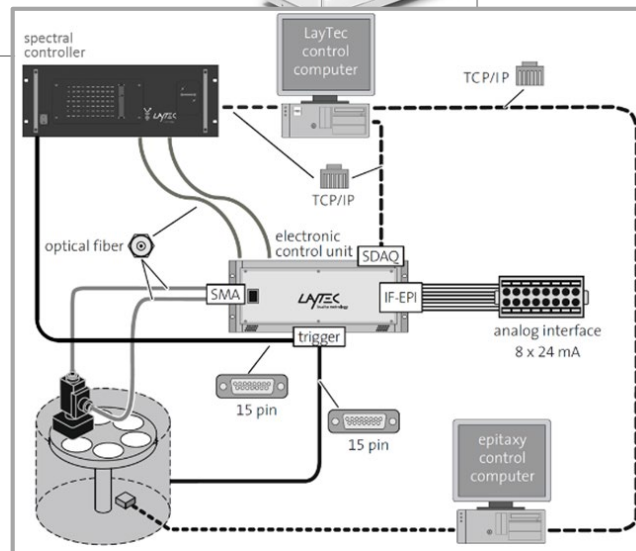
Process Module



8 x 6 inch



In-situ tool



This success is supported by recent advances in in-situ metrology:

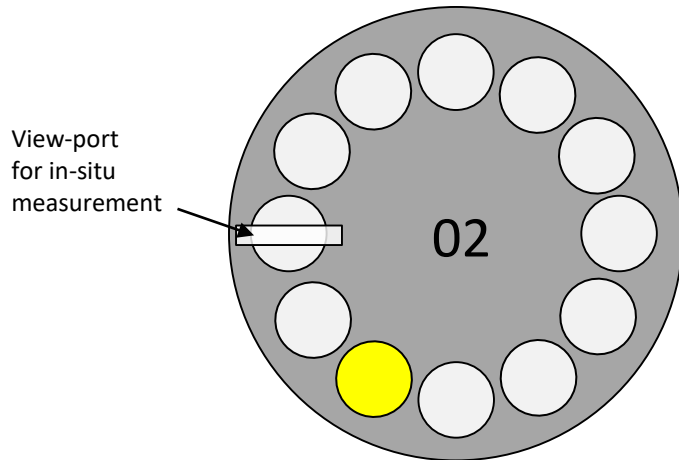
- Highly precise measurement of growth rates even for very thin layers in sophisticated multi-layer structures
- Recipe controlled automated in-situ data analysis, synchronized to epi recipe, interfaced to MES
- Metrology based feed-forward of wafer temperature for satellite rotation control in long and complex device runs

How to measure thin layers in a multi-wafer reactor?

Example: DBR interface layers in 940nm VCSEL

6 ... 15nm graded AlGaAs, typical growth times of 12 ... 30s

Typical susceptor rotation: 10 rpm, 12x3" configuration



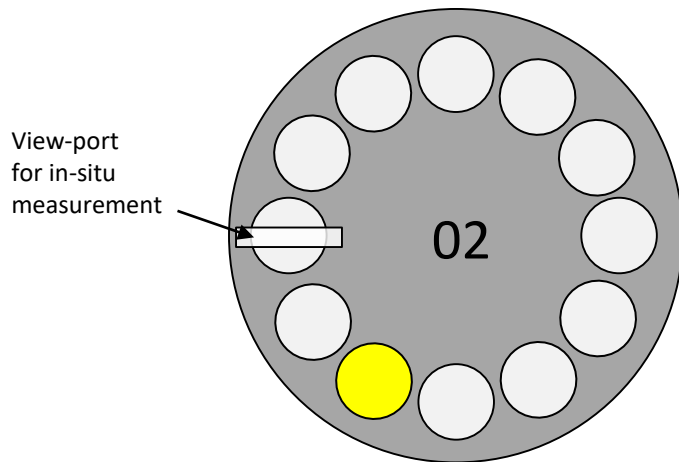
= Data acquisition every 6s
= 2 data points in 12s of growth
for a single wafer ... not enough!

How to measure thin layers in a multi-wafer reactor?

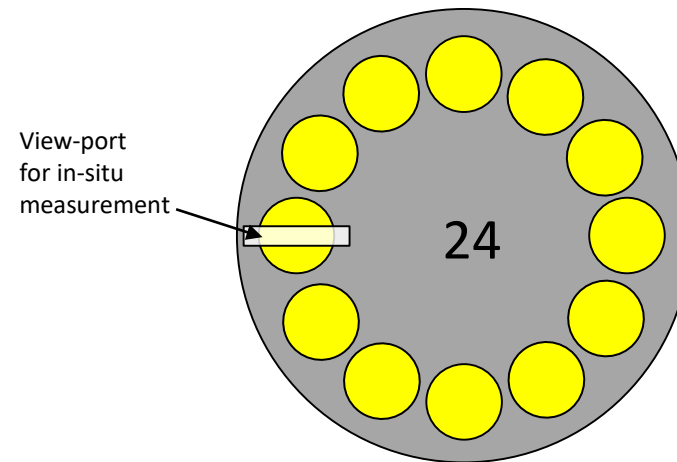
Example: DBR interface layers in 940nm VCSEL

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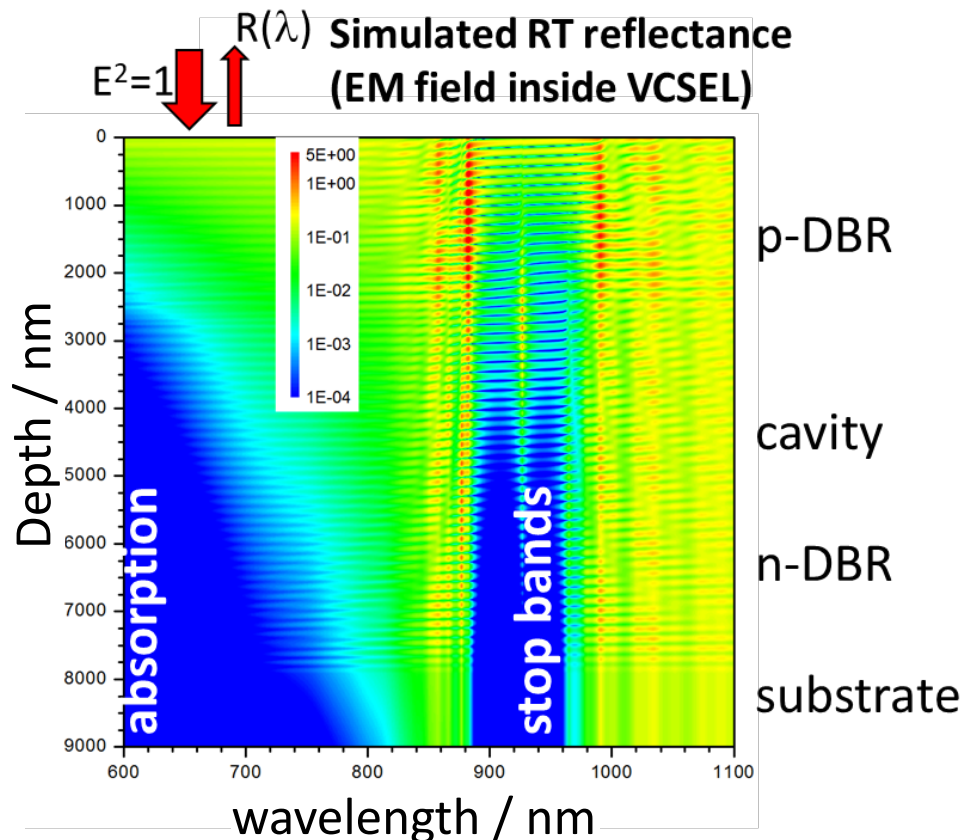
with „merged data“:
= data acquisition every 0.5s
= **24 data points in 12s of growth**

Merged dataline mode: A must for nm-scaled layers

Can we consider all wafers to be identical?

Yes, if we use the right wavelength!

Analysis of light penetration depth



$$\lambda > \lambda_{E0}: k \sim 0$$

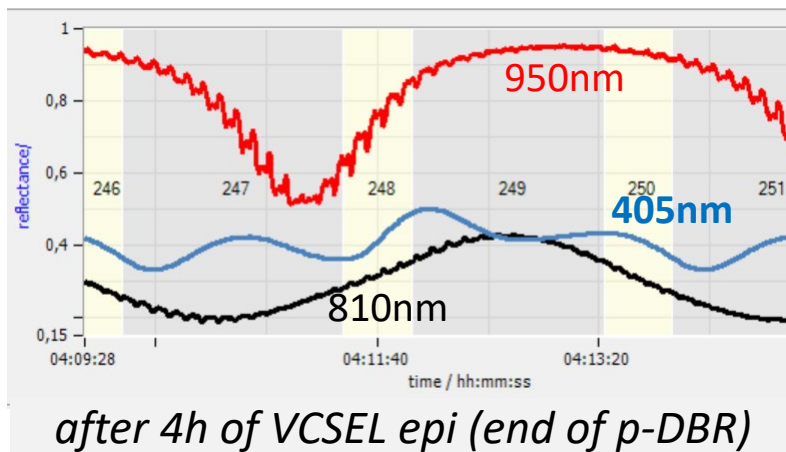
- light penetrates all of the complex layer structure
- tiny differences (wafer-to-wafer) accumulate
- merged datalines are getting „noisy“

$$\lambda < \lambda_{E0}: k > 0$$

- light penetrates the uppermost layers only
- growth highly uniform
- cutting-edge S/N of in-situ reflectance

Wavelength selection for high-accuracy growth rate monitoring of thin layer

- Longer wavelength penetrate through whole stack = wafer-to-wafer differences accumulate
- Shorter wavelength are sensitive to uppermost layer(s) only



Data: EpiCurveTT VCSEL at Aixtron G3 11x3"/1x4" (Jenoptik)

Experimental proof in AIX G3

← long wavelength („noisy“)

← short wavelength (no „noise“)

Use short wavelength for growth rate monitoring of very thin layers

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Current metrology challenges for VCSEL/DBR/SESAM

„Standard“ requirements

e.g. for **edge emitting lasers**

Growth rate = 0.500 ± 0.005 nm/s $\Rightarrow \sim \pm 1\%$

Today's advanced requirements

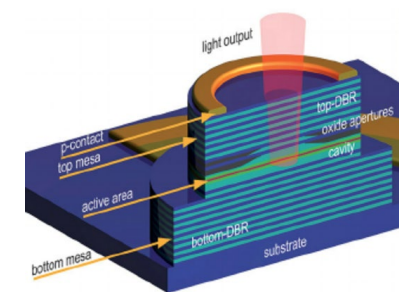
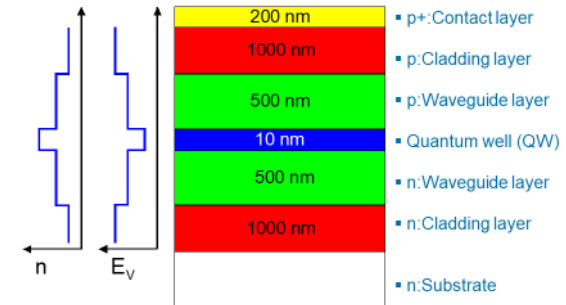
e.g. for **VCSEL** emission wavelength (940 ± 1)nm

Growth rate = 0.5000 ± 0.0005 nm/s $\Rightarrow \sim \pm 0.1\%$

Tasks for in-situ metrology:

- Accuracy in growth rate measurement
- integration into MOCVD for advanced process control (such as feed-forward control)

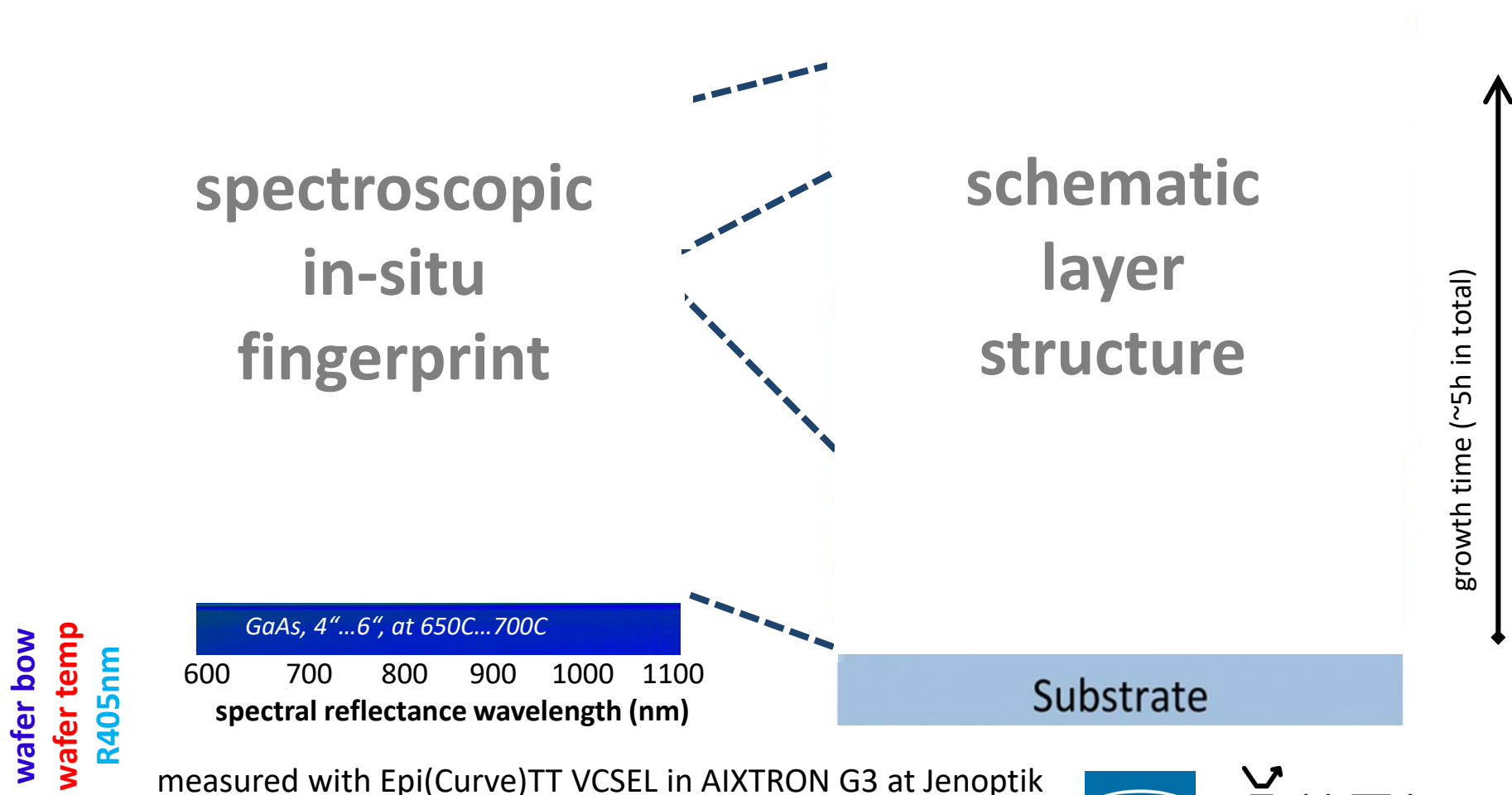
VCSEL	<u>v</u> ertical <u>c</u> avity <u>s</u> urface <u>e</u> mitting <u>l</u> aser
DBR	<u>d</u> istributed <u>B</u> ragg <u>m</u> irror
SESAM	<u>s</u> emiconductor <u>s</u> aturable <u>a</u> bsorber <u>m</u> irrors



- >100 layers; >5μm stack
- thin layers (DBR, MQW)
- graded interfaces in DBRs

Example of in-situ metrology of a VCSEL structure

Goal: reliable prognosis of device properties by in-situ spectral reflectance

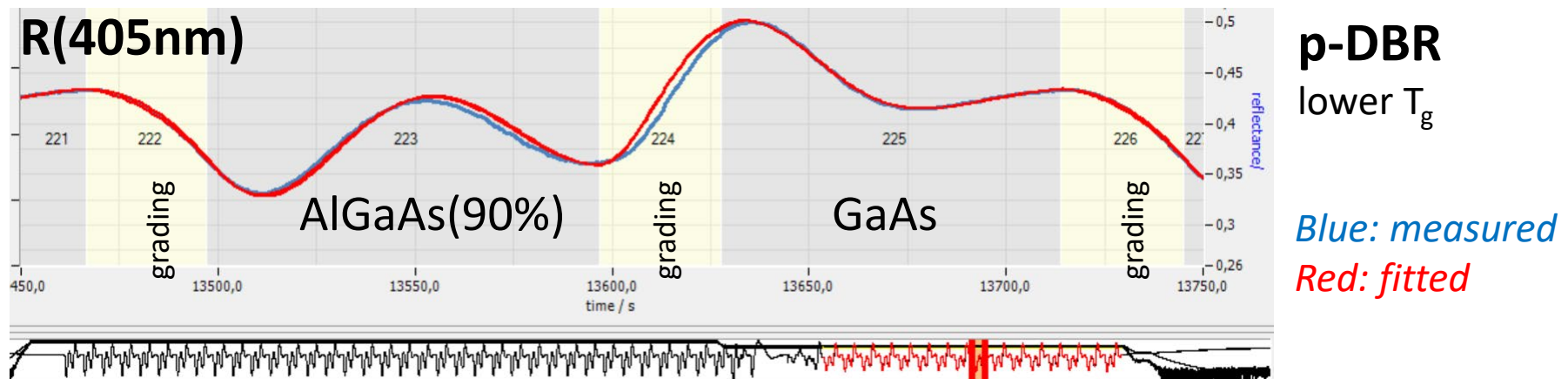


measured with Epi(Curve)TT VCSEL in AIXTRON G3 at Jenoptik

Example 1: Interface grading in 940nm VCSEL DBR

Approach:

model-based fit of measured reflectance curves for growth rate analysis



slow grading (30s)

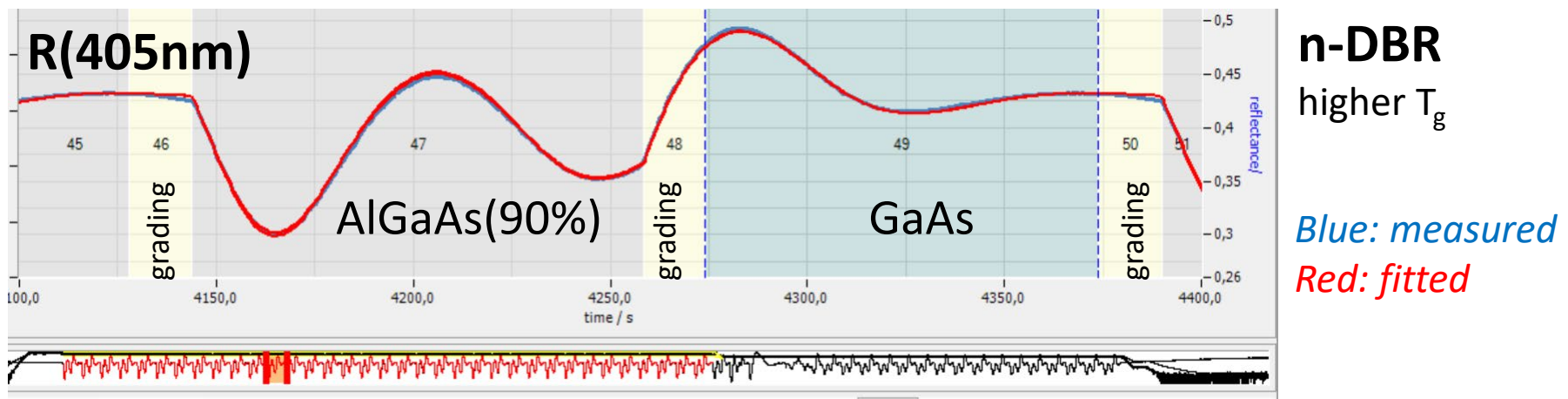
Model: linear grading

Good agreement with linear model

Example 1: Interface grading in 940nm VCSEL DBR

Approach:

model-based fit of measured reflectance curves for growth rate analysis



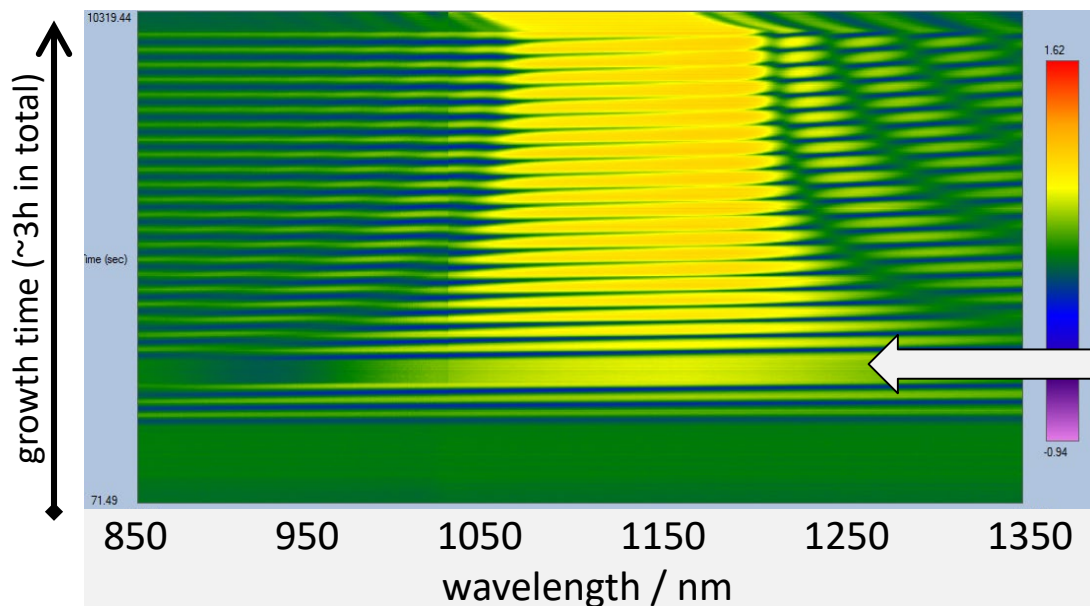
Fast grading (16s)

Model: no grading

Linear change in TMG/TMA gas-flow not always leads to linear grading in x_{AlGaAs}

Example 2: SESAM (1030±1)nm – feed-forward control

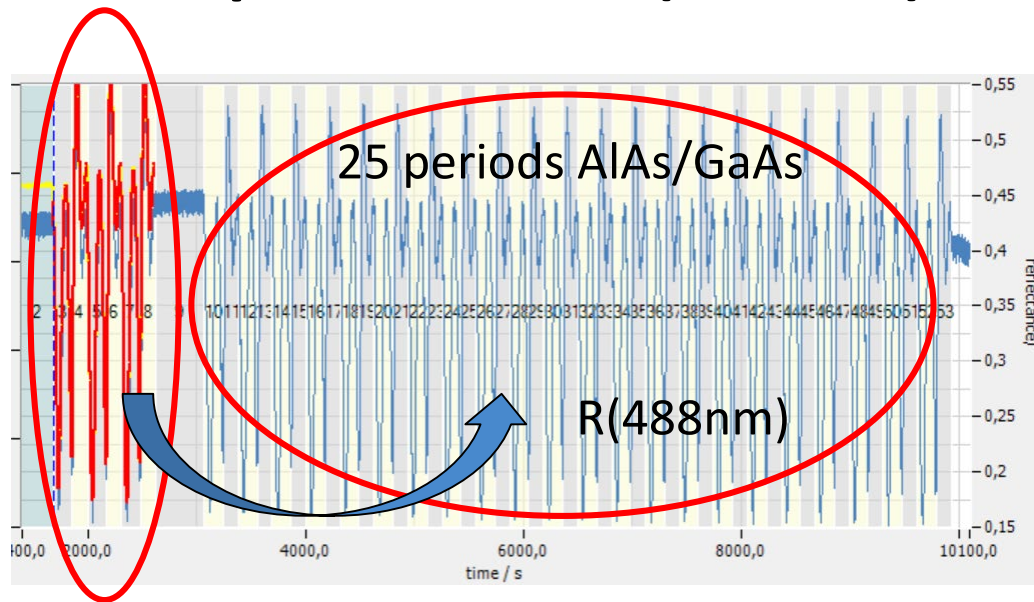
- 25 pairs of GaAs/AlAs
- Full load in AIXTRON G3
- DBR Stop-Band: 990-1090nm (RT); 1030-1200nm (high T, shifted)
- Monitored by wide spectral range version (488, 633, 700-1500nm) of EpiCurveTT VCSEL



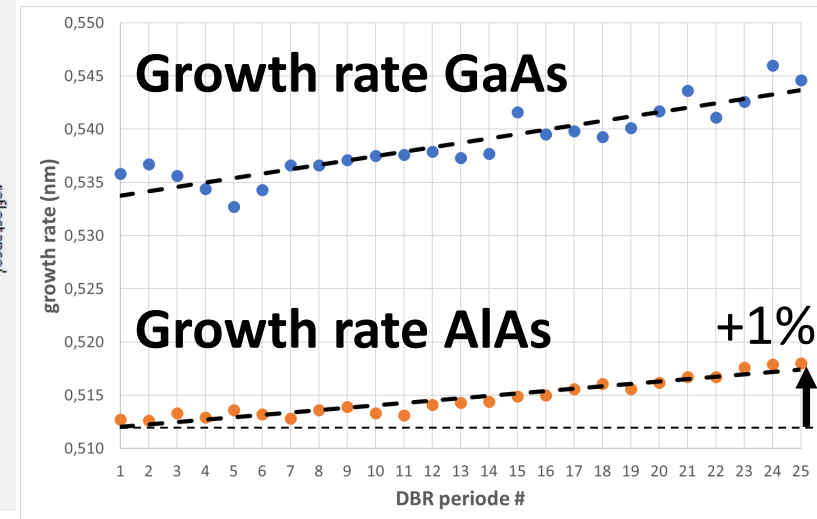
Spectral reflectance fingerprint (800-1350nm, ~3h of epi, cool-down wavelength shift is seen)

Epi pause - for 6-layer growth rate analysis and recipe feed-forward update

Example 2: SESAM (1030±1)nm – feed-forward control



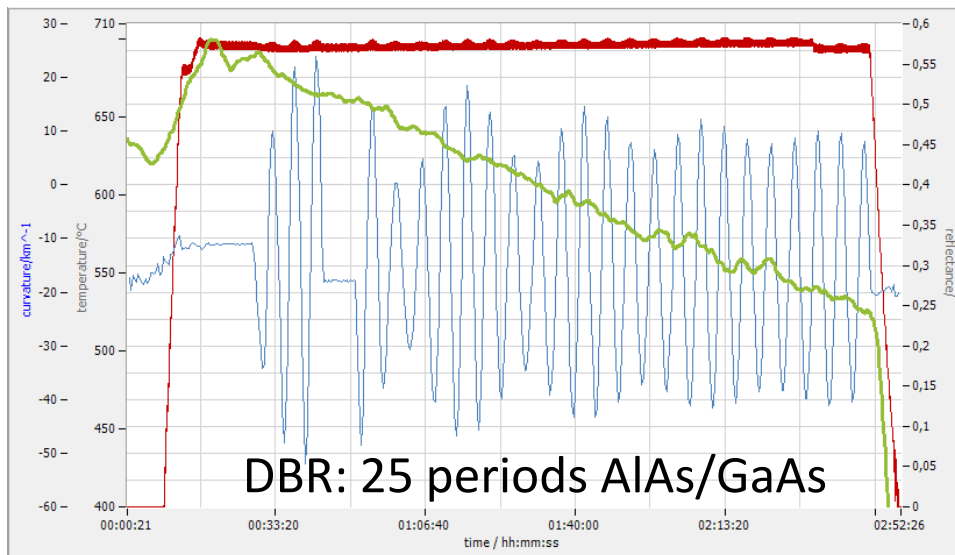
- Determine growth rates of GaAs and AlAs during first 3 DBR periods
- Transmit growth rate to growth system
- Update growth times in recipe („feed forward“)
- grow remaining 22 periods



- Detailed analysis of in-situ data show linear increase of growth rates over 25 periods
- Tiny effect, but important
- Must be taken into account to achieve desired accuracy

Example 2: SESAM (1030±1)nm – feed-forward control

Why is growth rate slightly changing during DBR?

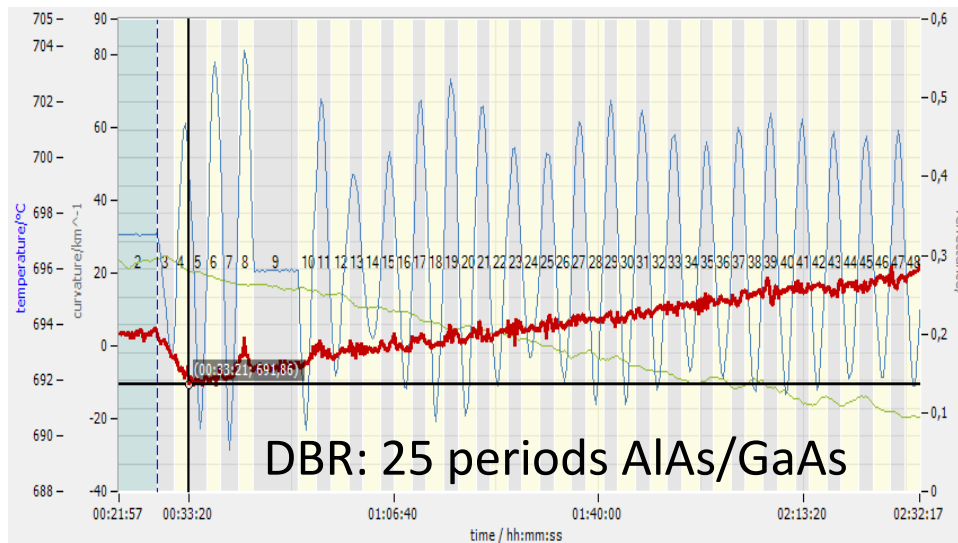


- Wafer is bowing during DBR growth (compressive strain in AlAs/GaAs stack)
- Thermal emission of wafer is reduced (growing DBR is covering GaAs band-edge wavelength) → reduced cooling by radiation
→ wafer temperature is increasing by ~4K
→ AIXTRON's AFF technology needed to compensate

True Temperature
Reflectance 950nm
Curvature

Example 2: SESAM (1030±1)nm – feed-forward control

Why is growth rate slightly changing during DBR?



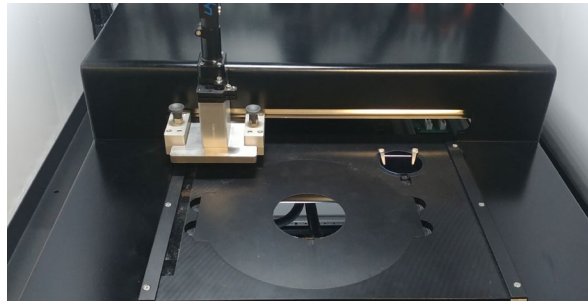
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- Thermal emission of wafer is reduced (growing DBR is covering GaAs band-edge wavelength) → reduced cooling by radiation → wafer temperature is increasing by ~4K → AIXTRON's AFF technology needed to compensate
- And other effects ...

True Temperature
Reflectance 950nm
Curvature

Example 2: Verification by ex-situ mapping

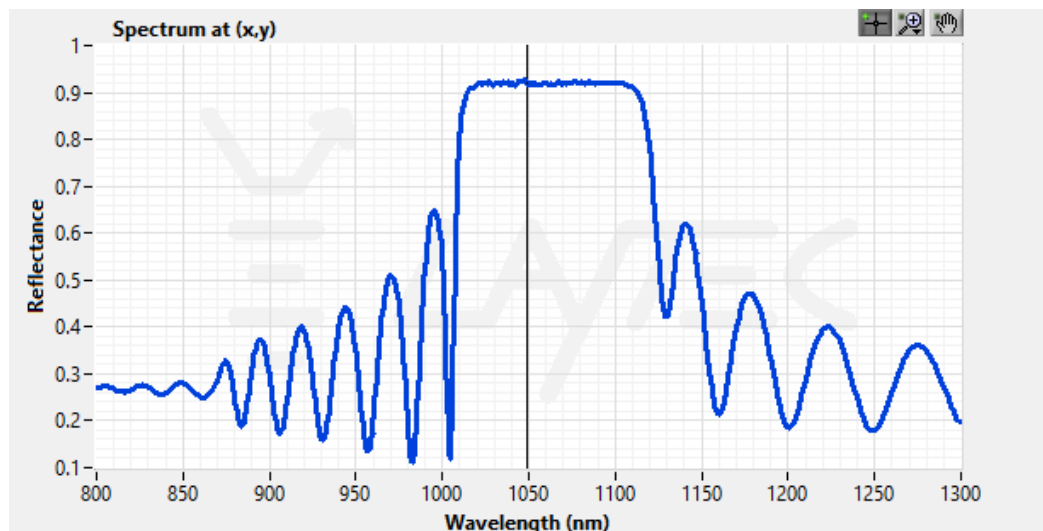


LayTec EPIX system



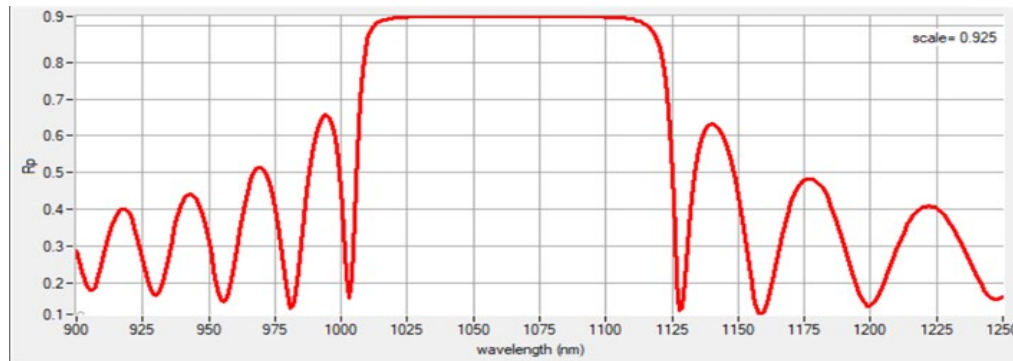
Mapping stage, 3" sample holder plate

Mapping station EPIX combines white light reflectance and PL (multi-head mapping)



SESAM DBR, center of wafer, white-light reflectance

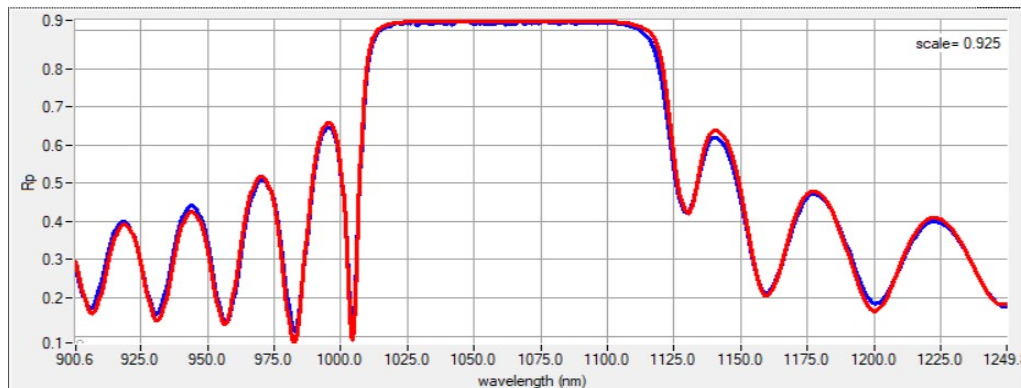
Example 2: Ex-situ growth rate analysis in wafer center



Calculated reflectance spectrum of ideal DBR would be highly symmetric

Growth rate $\text{GaAs} = 0.497 \text{ nm/s}$

Growth rate $\text{AlAs} = 0.580 \text{ nm/s}$



Blue: Measured DBR spectrum; asymmetric

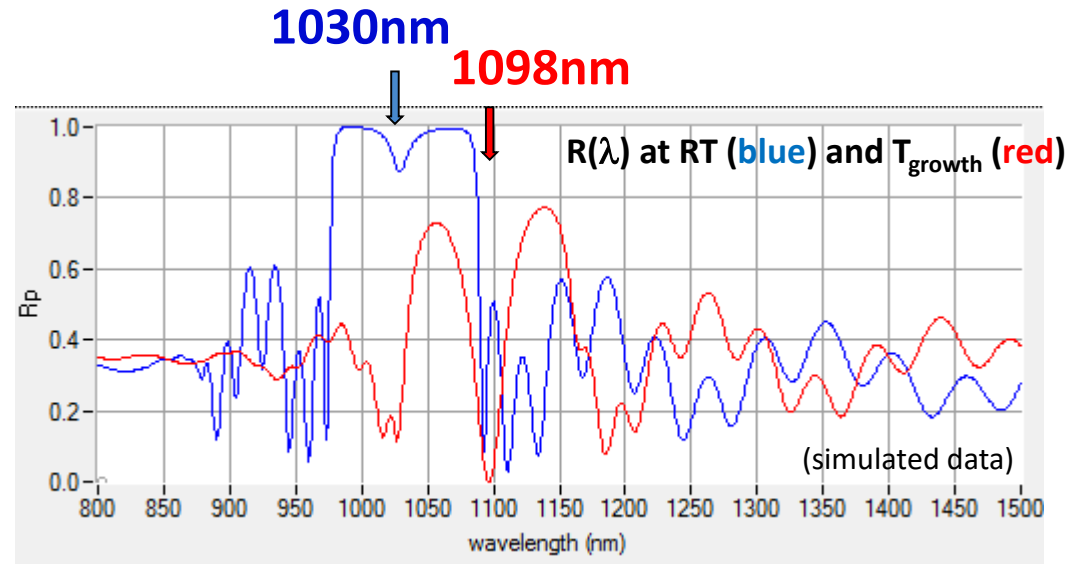
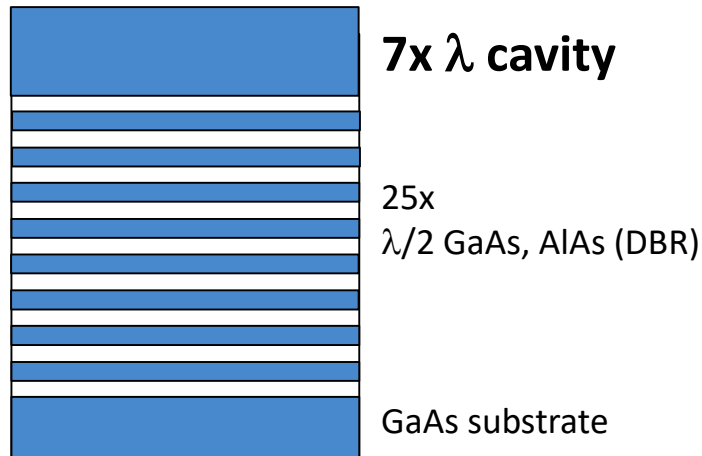
Red: Analytic model based on in-situ measured growth rates with linear increase

Growth rate $\text{GaAs} = 0.4955 \text{ nm/s} \rightarrow 0.4990 \text{ nm/s}$ (+1% from start of DBR to end of DBR)

Growth rate $\text{AlAs} = 0.5769 \text{ nm/s} \rightarrow 0.5839 \text{ nm/s}$ (+1% ...)

Excellent agreement to measured ex-situ reflectance spectrum in wafer center

Example 3: cavity end-point detection for 1030nm SESAM



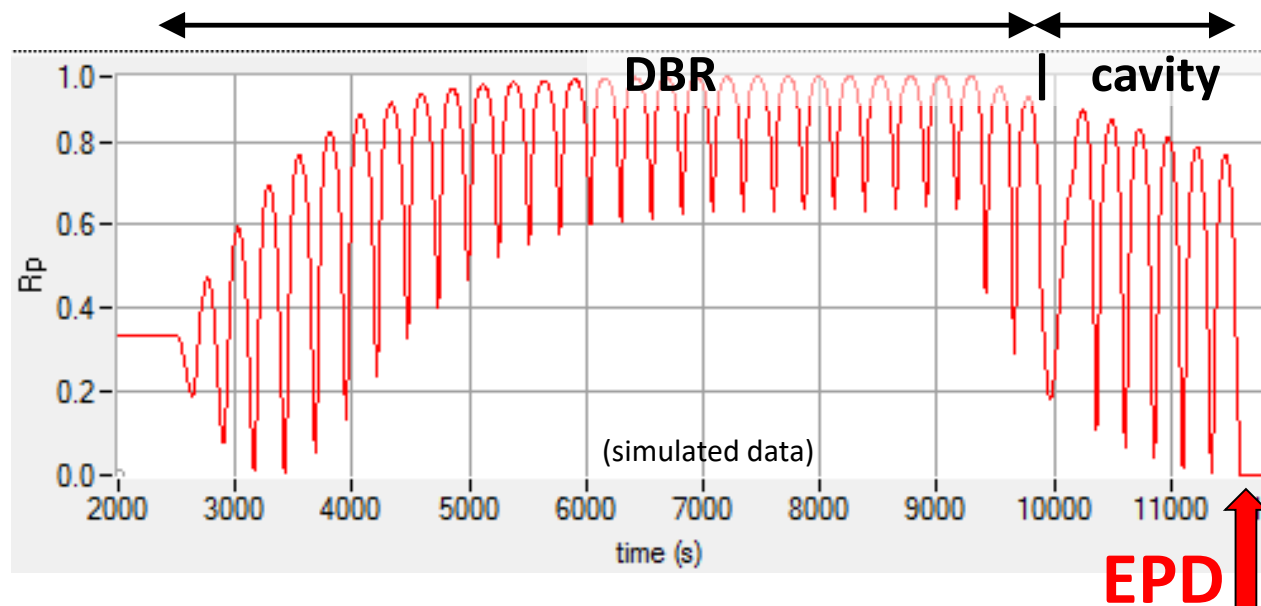
Goal: Grow cavity with thickness of exactly 7λ for $\lambda=1030\text{nm}$

Problem: At growth temperature cavity dip and stop band are shifted to longer wavelength
i.e. end-point control at 1030nm is useless

Solution: Select shifted wavelength of cavity resonance at T_{growth} for end-point detection (EPD) of cavity thickness: 1098nm

Example 3: cavity end-point detection for 1030nm SESAM

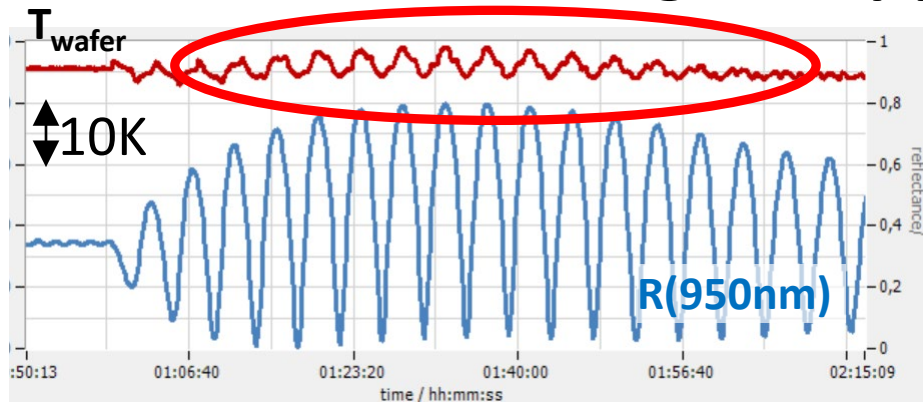
1098nm in-situ transient



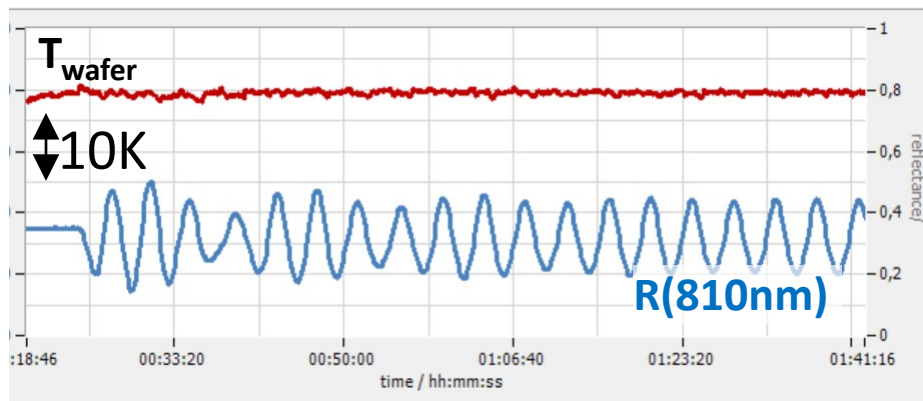
- Monitor reflectance at 1098nm
- Stop growth when reflectance curve goes through 7th minimum

- Full spectroscopic measurement allows free choice of ideal wavelength for end-point detection (EPD)
- $\pm 1\text{nm}$ accuracy in cavity dip – possible by EPD

940nm VCSEL – adding a 2nd pyrometry wavelength

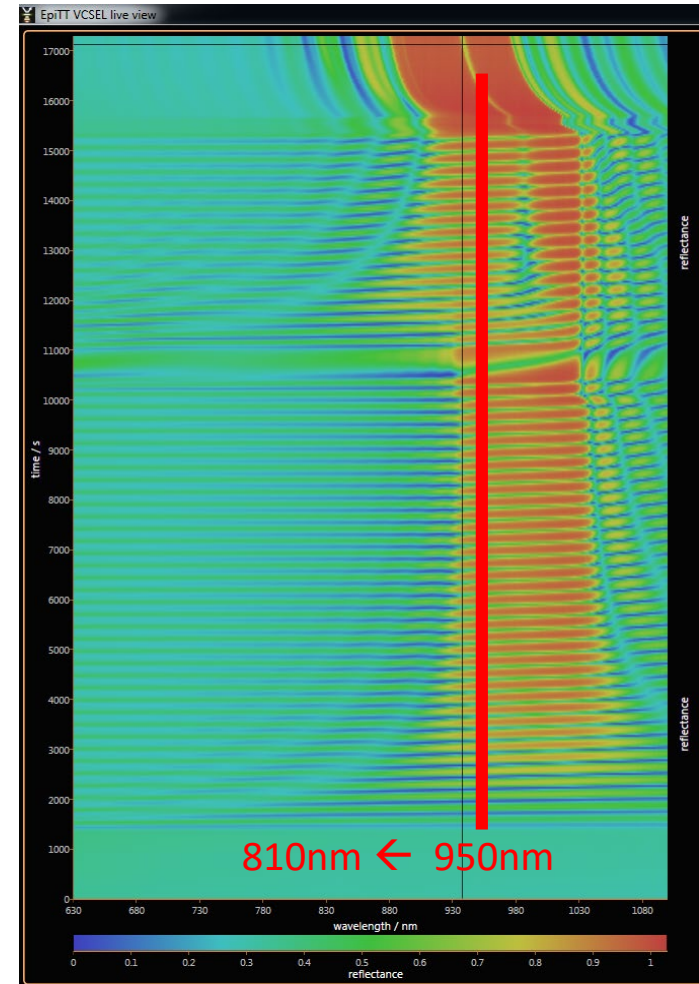


950nm pyro: wafer's thermal radiation blocked by DBR ($\epsilon=1-R < 20\%$) \rightarrow strong artifacts in T_{wafer}



Second 810nm pyrometer:

wafer's thermal emissivity ϵ always $> 60\%$
 \rightarrow wafer temperature free of FPO artifacts



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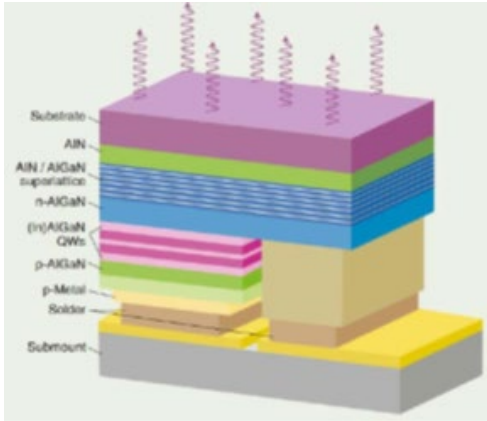
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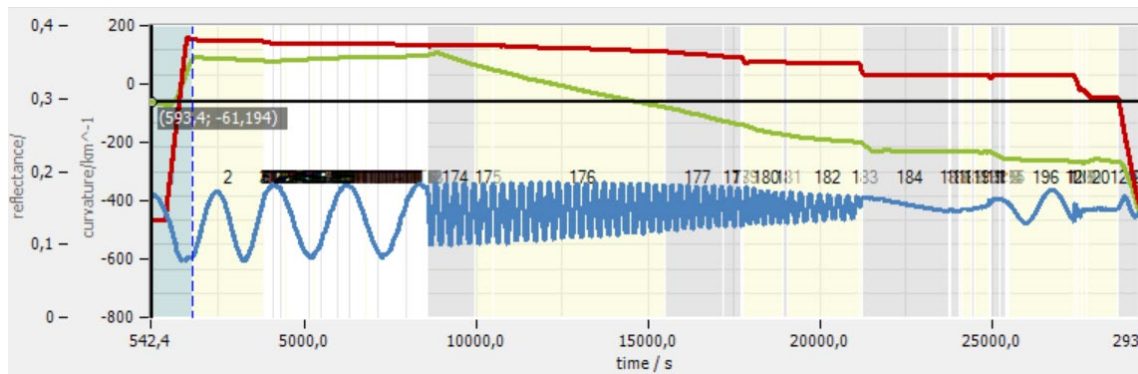
Summary and outlook

In-situ metrology for epitaxy of UV-C LEDs



- Growth on sapphire/AlN template
- 8h long epi; low growth rates for smoother interfaces
- two-step Epi:
 - template growth in AIXTRON G3
 - LED-structure in 6x2" CCS
- Total thickness: 1.5 μm AlN template + 5-6 μm of LED
- 85 period GaN/AlN superlattice for defect reduction

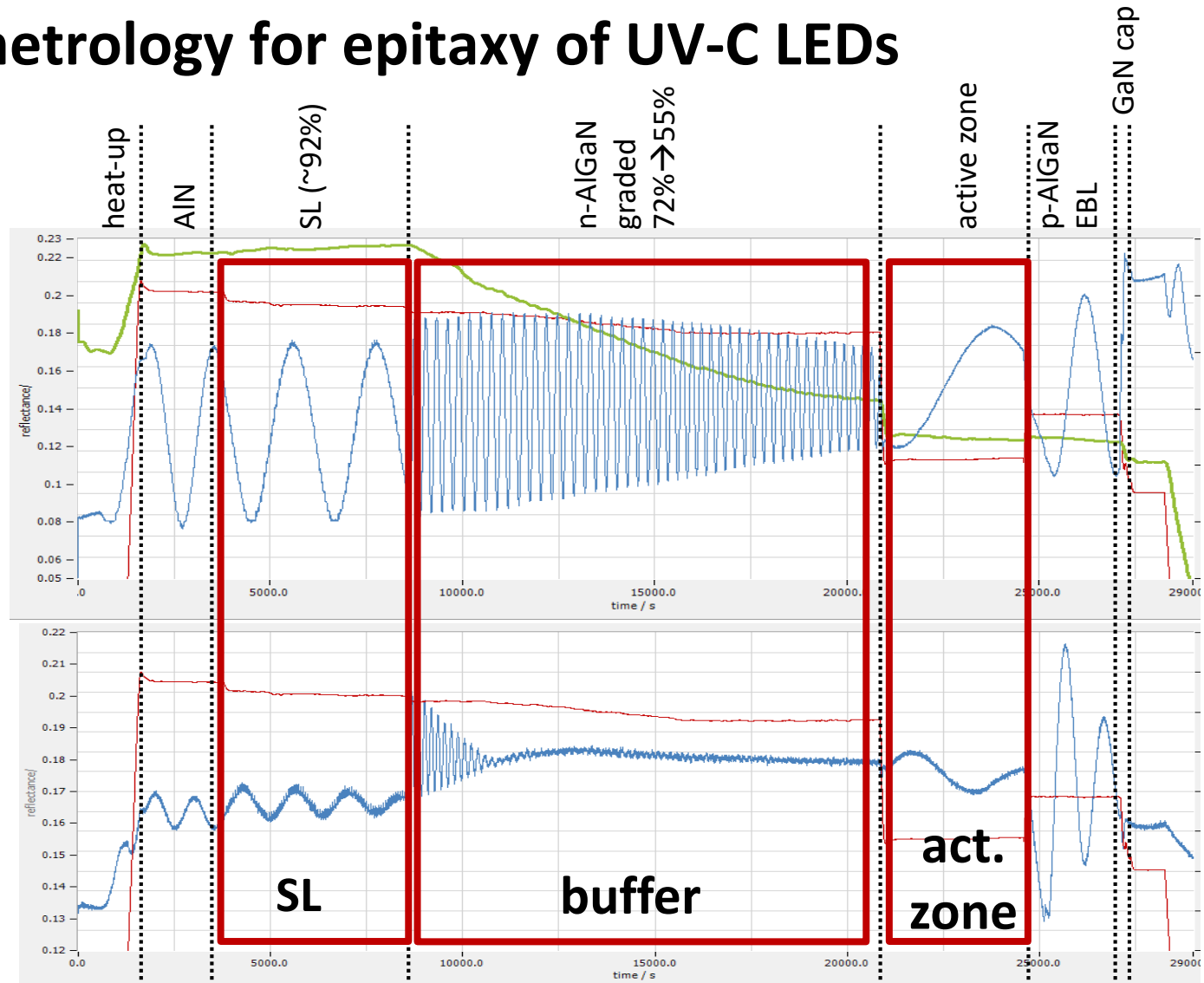
4-wavelength reflectance monitoring (280/405/633/950nm) for providing access to all layer thicknesses



In-situ metrology for epitaxy of UV-C LEDs

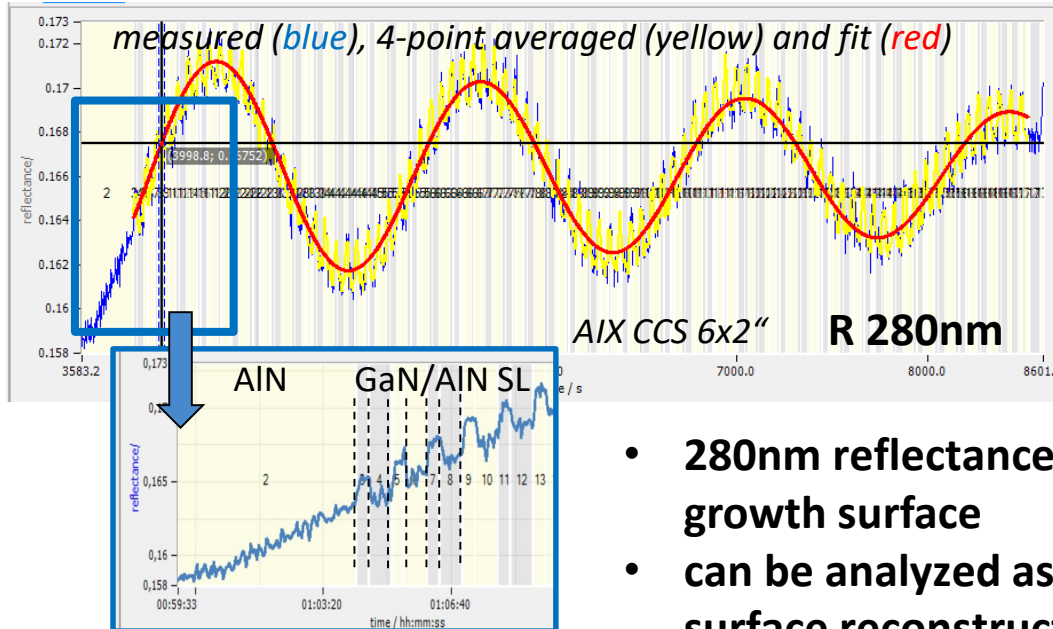
R 405nm
curvature
temperature

R 280nm
curvature
temperature



In-situ metrology for epitaxy of UV-C LEDs: Superlattice

- GaN/AlN SL is decisive at beginning of the UV LED epitaxy for defect reduction
- 85 periods, each single layer in the range of $\sim 1\text{nm}$

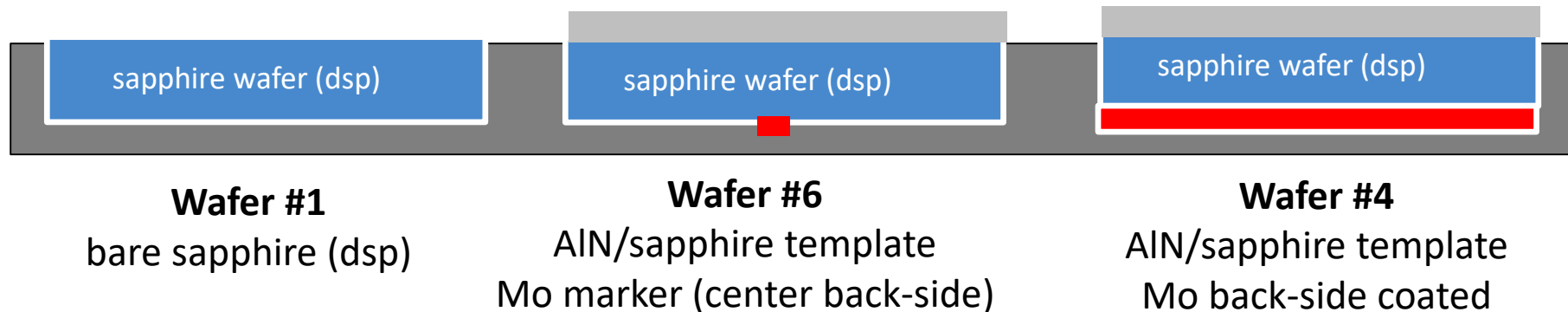


← fitting the 280nm reflection during SL growth yields SL total layer thickness of 201nm (red line)

- 280nm reflectance shows gas phase effects to the growth surface
- can be analyzed as a SPA experiment sensing the surface reconstruction changes from Al-rich \rightarrow Ga-rich \rightarrow Al-rich \rightarrow ...

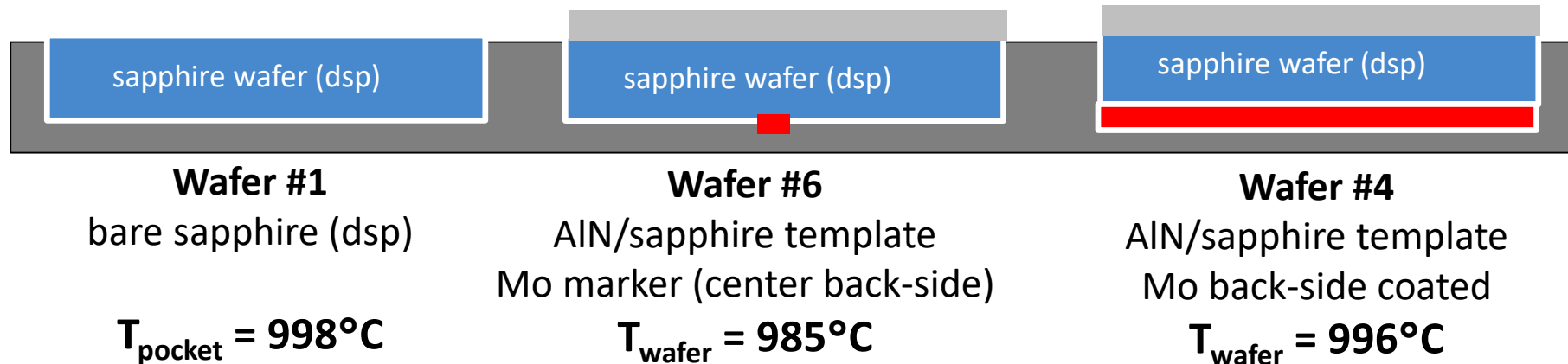
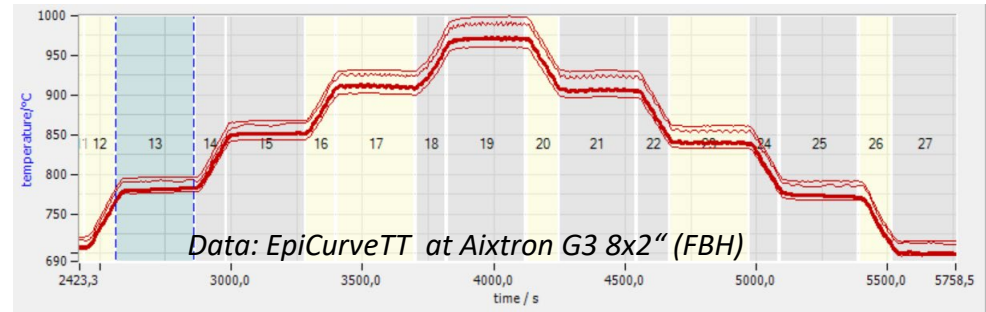
UV LEDs – so far no in-situ access to wafer temperature

- Fully NIR transparent substrates and layers do not allow pyrometry of wafer temperature - only pocket temperature measurement
- Molybdenum back-side coating is used for getting access to T_{wafer} of AlN/sapph templates at start of UV-LED process
- This is work in progress ...



UV LEDs – so far no in-situ access to wafer temperature

- Heating run with three different wafers
- In-situ temperature measurement
- Approach will help studying wafer temperature during UV-LED epi



- The AlN template wafer temperature at begin of UV-LED growth is 13K below pocket (graphite/SiC) temperature
- Full Mo coating of sapphire back-side improves the heat-transfer

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Summary and Outlook

- We have developed new methods and procedures for measuring the growth rates of thin layers in highly complex device structures
- high-yield manufacturing of current cutting-edge devices can only be facilitated by close integration of in-situ metrology into the MOCVD tools
- Grading of ternary layers in DBR-like structures can be analyzed in-situ
- Ex-situ mapping of Epi uniformity achieves a new level of accuracy by feeding in the results of in-situ analysis
- Feed-forward control schemes allow endpoint detection for DBR and cavity
- Precision in in-situ reflection gives access now to surface reconstruction changes during growth
- Challenges in wafer temperature sensing for VCSELs processes have been solved
- Wafer temperature in UV LED epi remains an open issue

Acknowledgement

The authors gratefully acknowledge the financial support by the Federal Ministry of Education and Research (BMBF) of Germany in the framework of “Zwanzig20” in the project “UV Power”



The authors gratefully acknowledge the financial support by the Federal Ministry for Economic Affairs and Energy (BMWi) of Germany in the project “MOCVD 4.2”

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Knowledge is key



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