# Metrology for MOCVD Processes - Latest Progress

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# Outline

- Metrology for MOCVD – a quick ride through some past milestones
- Current metrology challenges (VCSELs, UV LEDs, Power Electronics)
- Latest metrology for VCSELs, DBRs, SESAMs
- UV-LEDs: in-situ metrology for high Al-containing III-Ns
- Wafer temperature sensing – latest: pHEMTs, VCSELs, UV-LEDs
- Summary & outlook

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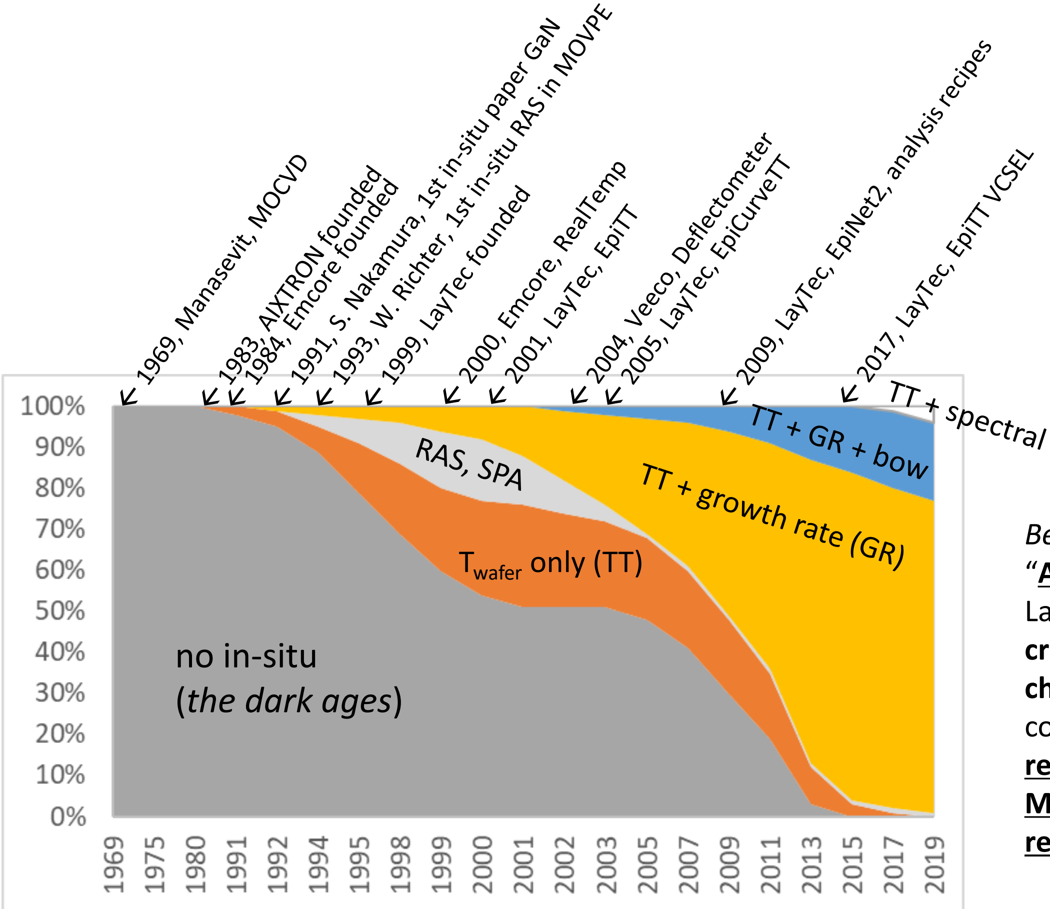
# In-situ Monitoring for MOCVD – a sketch of historic development




*Ben Stevens et al. (IQE), CSManTech, May 2019:*
"**<u>All VCSEL reactors at IQE use a LayTec EpiTT</u>** … The LayTec system also **enables characterization of critical layers in a VCSEL that could not be characterized by traditional means** or would require complicated modelling. **<u>Through use of analysis recipes the required analysis can be loaded into the MES before the wafers are even unloaded from the reactor</u>**."



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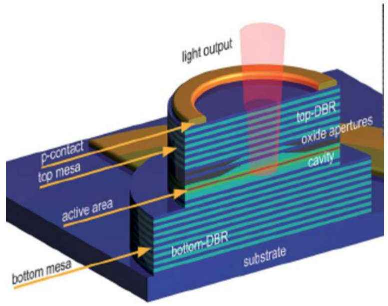
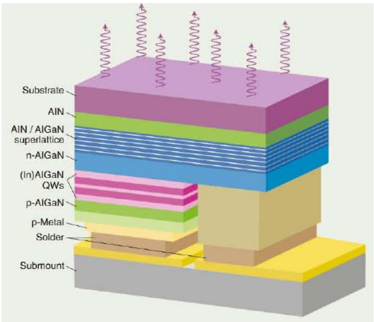
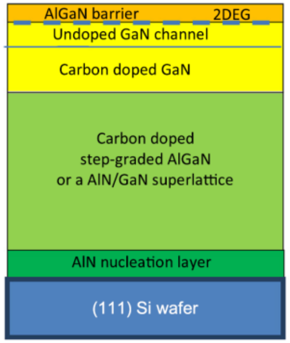
- **Current metrology challenges (VCSELs, UV LEDs, Power Electronics)**
- Wafer temperature sensing – latest progress
- Advanced in-situ analysis – new algorithms
- Spectral in-situ sensing for VCSELs, DBRs, SESAMs
- Combining nondestructive in-situ and ex-situ metrology
- Summary & outlook

# Current metrology challenges




## VCSEL on GaAs

- >100 layers; >5µm stack
- 0.1% accuracy in growth rate
- pyrometry blocked by DBR
- $x_{AlGaAs}$ for oxide aperture
- **graded interfaces** in DBRs
- nm-scaled layers (MQW, grading)

## UV-C LED on sapphire

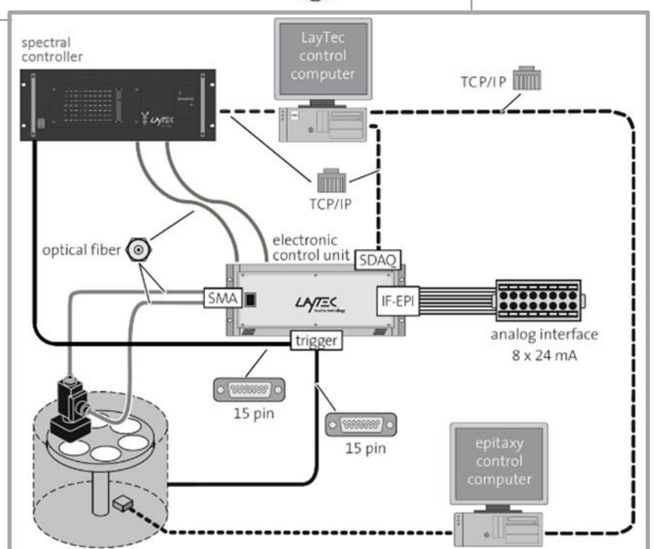
- 2-step epi (AlN/sapph + LED)
- >3µm stack, all layers k=0
- no access to $T_{wafer}$
- **surface roughness ($x_{AlGaN}$ >0,5)**
- High strain (AlGaN on AlN)
- nm-scaled layers (MQW, SL, EBL)

## GaN/Si Power HEMT

- Large wafers + large bow
- Pyrometry: GaN is ARC on Si, 40% oscillations in emissivity
- >3µm stack, all layers k=0
- **Wafer temperature during AlGaN barrier growth** is extremely critical

**These 3 very different device structures have in common: >5 hours of Epi; wafer temperature sensing is very difficult and high-yield manufacturing is not possible without in-situ metrology.**

# Currently there is a clearly market leading MOCVD tool for VCSELs and GaN/Si HEMTs: AIXTRON's G4/G5


**This success is supported by recent advances in in-situ metrology:**

- Metrology based feed-forward of wafer temperature for satellite rotation control in long and complex device runs.
- Highly precise measurement of growth rates even for very thin layers in sophisticated multi-layer structures.
- Recipe controlled automated in-situ data analysis, synchronized to epi recipe, auto feed-forwarded to MES.

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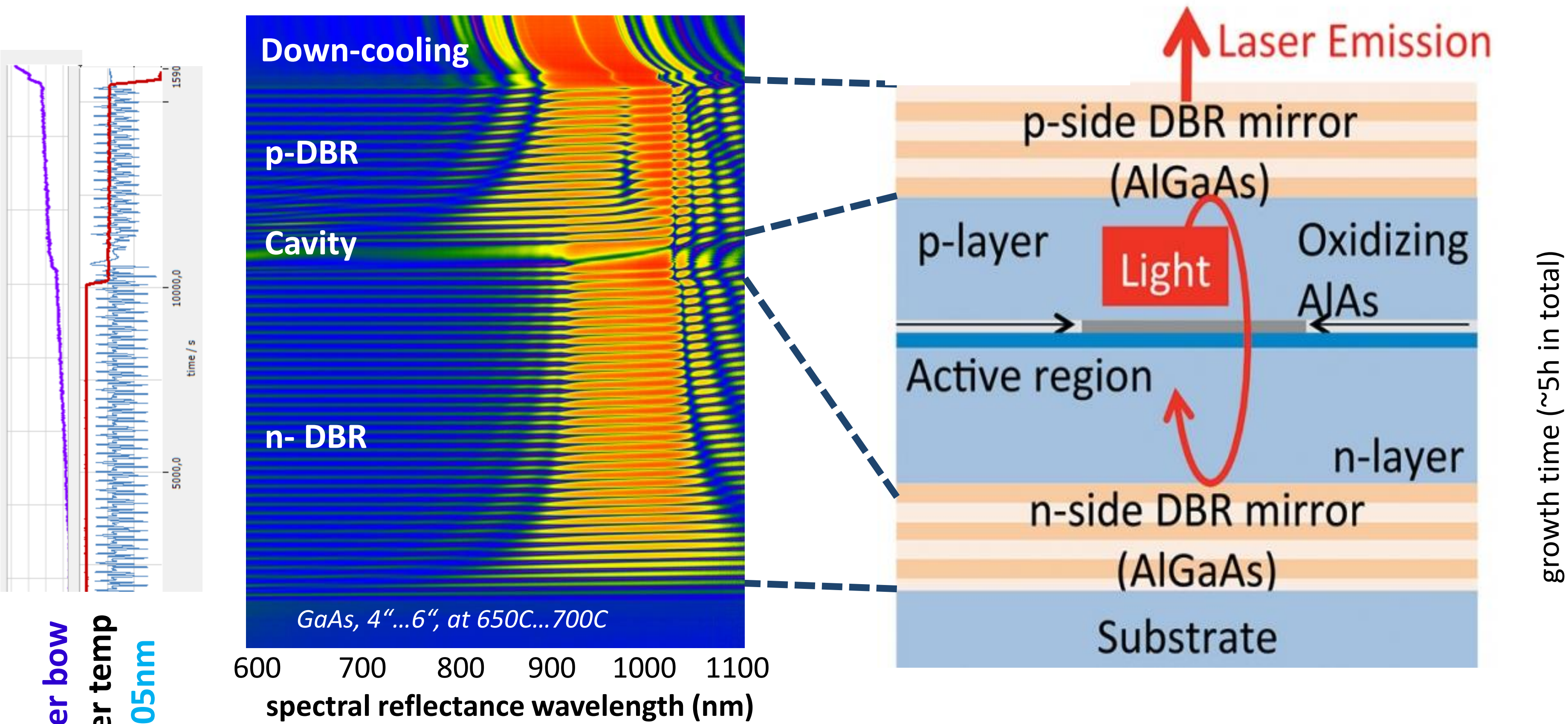
# VCSEL MOCVD: reliable prognosis of device properties by in-situ spectral reflectance – Epi(Curve)TT VCSEL




*Data: EpiCurveTT VCSEL at Aixtron G3 12x3" (Jenoptik)*

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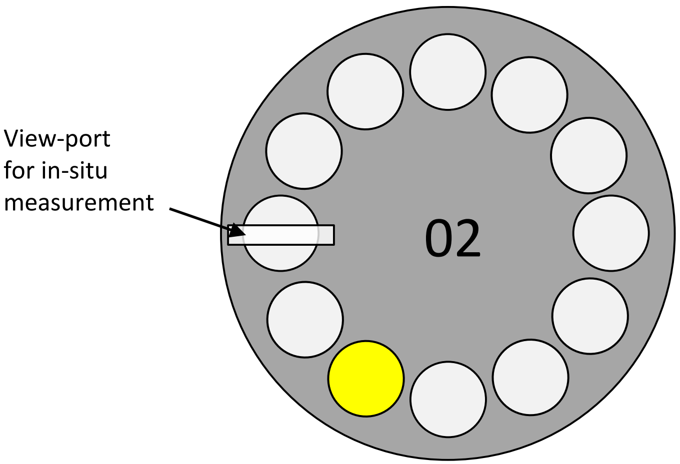
# nm-scaled layers in G3/G4 planetary reactors

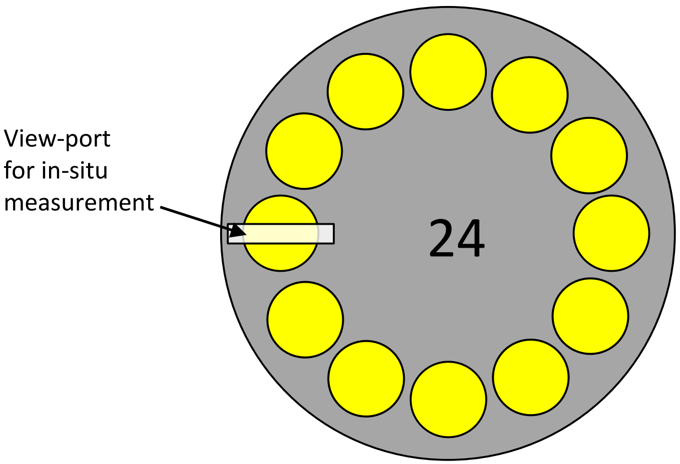
**Example: DBR interface layers (graded) in 940nm VCSELs:** 6 … 15nm graded AlGaAs, typical growth times of 12 … 30 seconds.

**10 rpm; Single Data-Line**




Data acquisition every 6s
**2 data points / 12s of growth**

**10 rpm, Merged Data-Line**




Data acquisition every 0.5s
**24 data points in 12s of growth**

**Merged Dataline Mode - a must for monitoring nm-scaled layers in G3/G4. Preferred: short-$\lambda$ (405nm) → surface sensitive!**



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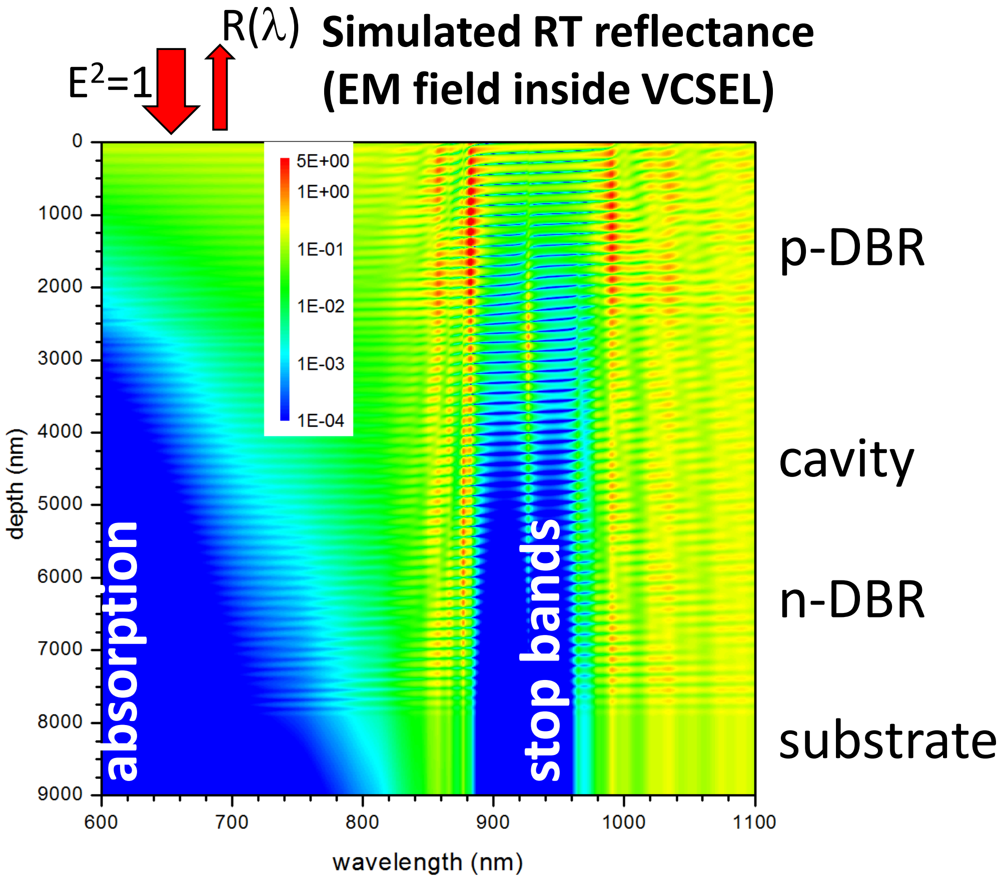
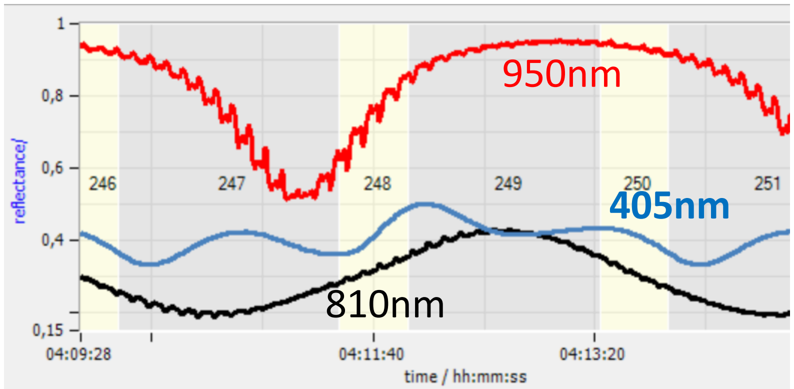
# Wavelength selection for high-accuracy growth rates in DBRs and MQWs → analysis of light penetration depth

**Simulated RT reflectance (EM field inside VCSEL)**




Color-Code = Lg-scale, normalized to incoming intensity of 1.0

$\lambda > \lambda_{E0}$: k~0 → light penetrates all the complex layer structure → tiny differences (wafer-to-wafer) accumulated → merged datalines are getting noisy.
$\lambda \ll \lambda_{E0}$: k>0 → light penetrates the uppermost layers only → cutting-edge S/N of in-situ reflectance.




*After 4h of VCSEL Epi (end of p-DBR)*

*Data: EpiCurveTT VCSEL at Aixtron G3 11x3"/1x4" (Jenoptik)*

**Use short-λ for GR of very thin layers!**

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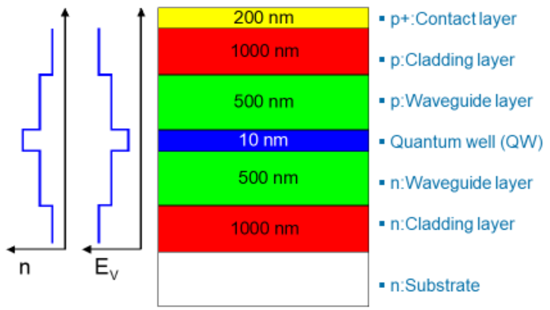
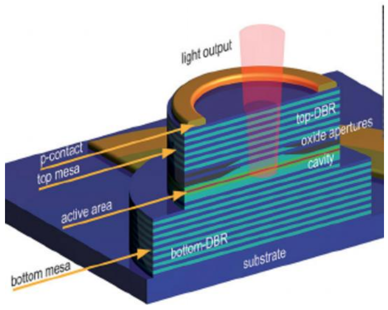
# Current metrology challenges

For **edge emitting lasers** the requirements are:
GR = 0.500 ± 0.005 nm/s **(~±1%)**



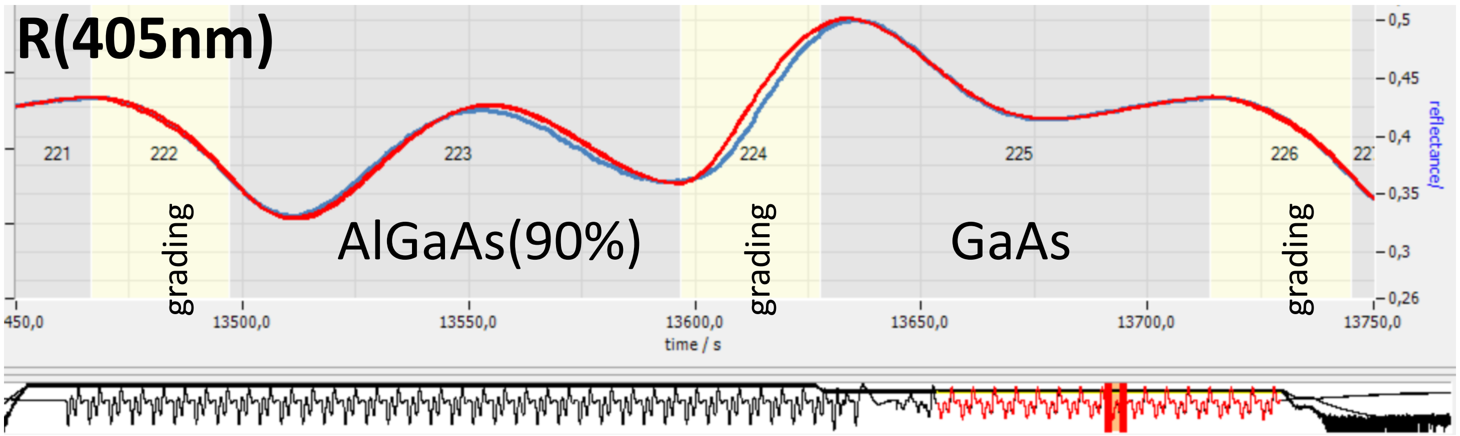

**VCSEL emission wavelength**
**940 ± 1 nm**
**means:**
**GR = 0.5000 ± 0.0005 nm/s (~±0.1%)**




**Task for in-situ metrology:**
- Accuracy in GR measurement!
- integration into MOCVD for feed-forward control (latest Aixact MOCVD control software)

- >100 layers; >5µm stack
- thin layers (DBR, MQW)
- graded interfaces in DBRs

# 940nm VCSEL DBRs – graded interfaces and GR accuracy




**p-DBR**

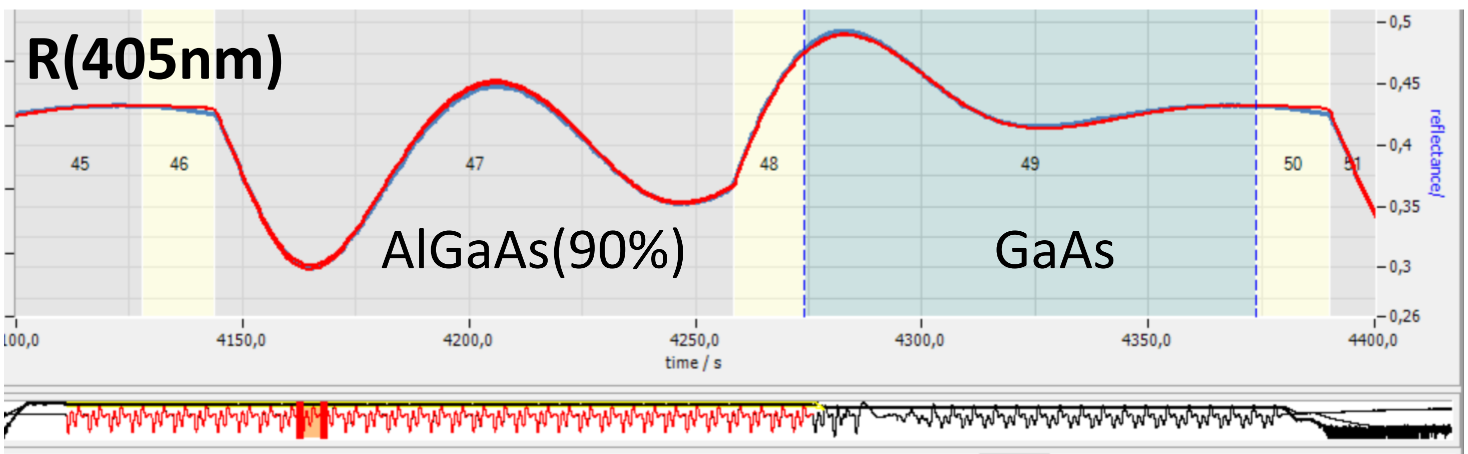
lower $T_g$

**slow grading (30s)**

Model: lin. grading

*Blue: measured*

*Red: fitted*




**n-DBR**

higher $T_g$

**fast grading (16s)**

Model: No Grading

*Blue: measured*

*Red: fitted*

**Linear change in TMG/TMA gas-flow → NOT always a lin. grading in $x_{AlGaAs}$**

**Growth rate (GR) fit: select correct <u>multi-layer</u> model!**



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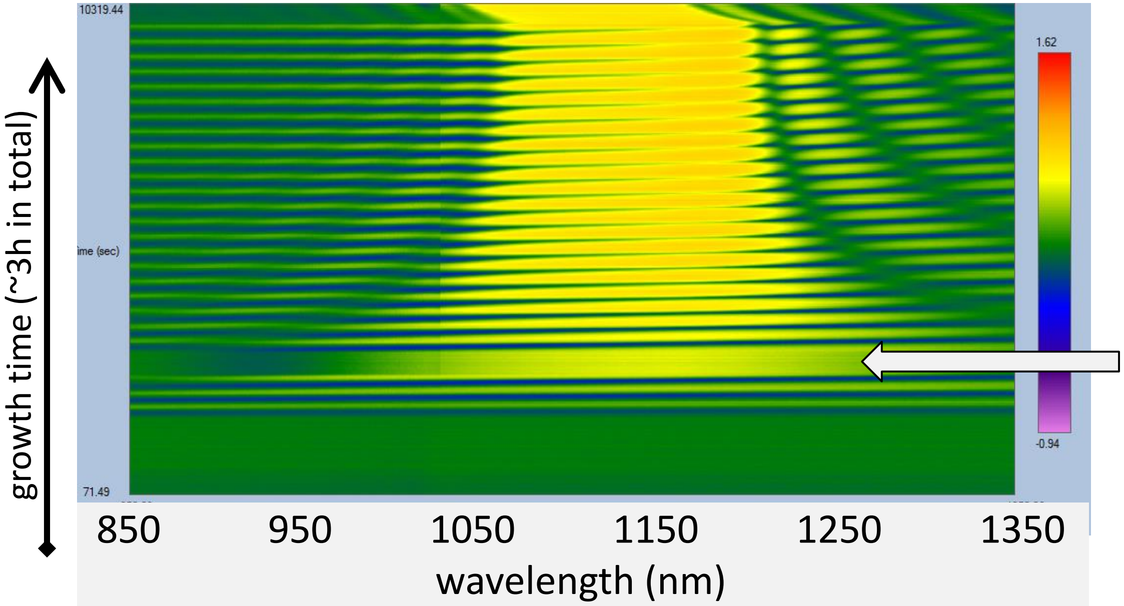
# SESAM DBR (1040nm ± 1nm) – Feed-Forward Control

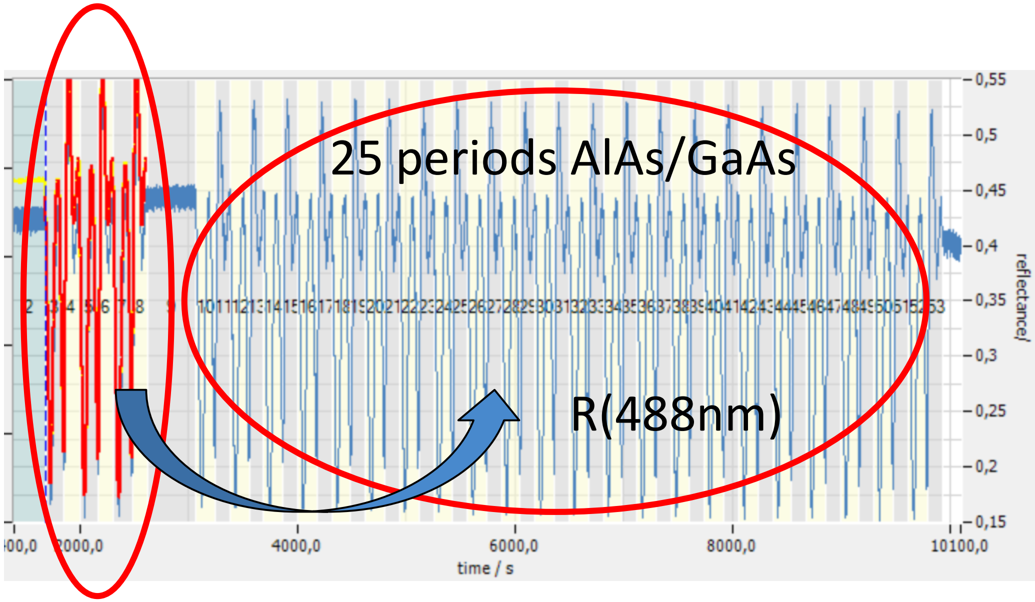
- 25 pairs of GaAs / AlAs
- Full load epi in AIXTRON G3
- DBR Stop-Band: 990-1090nm (RT); 1030-1200nm (GT, up-shifted)
- Monitored by wide spectral range version (488, 633, 700-1500nm) version of EpiCurveTT VCSEL

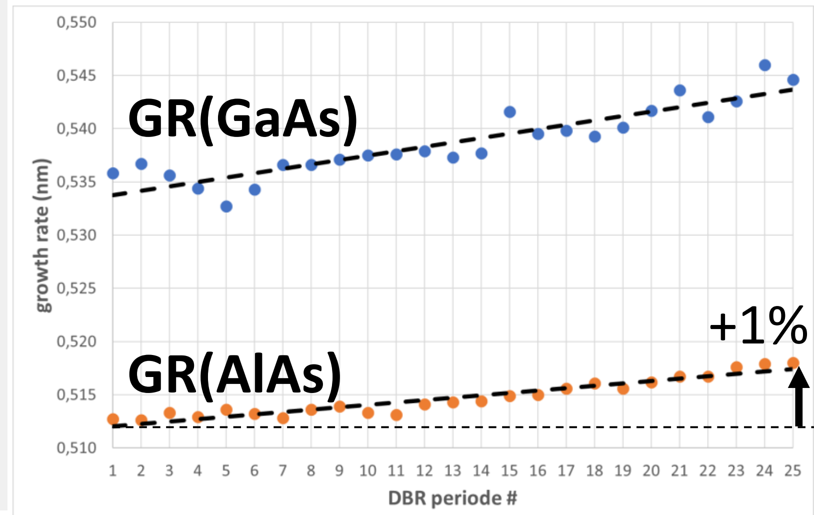



*Spectral reflectance finger-print (800-1350nm, ~3h of epi, cool-down wavelength shift is seen)*

***Epi pause -*** *for 6-layer GR analysis and recipe feed-forward update*

# SESAM DBR (1040nm ± 1nm) – Feed-Forward Control




<u>First 3 DBR periods:</u> growth rates (GaAs, AlAs) in-situ measured: multi-layer, graded interfaces (if so)!

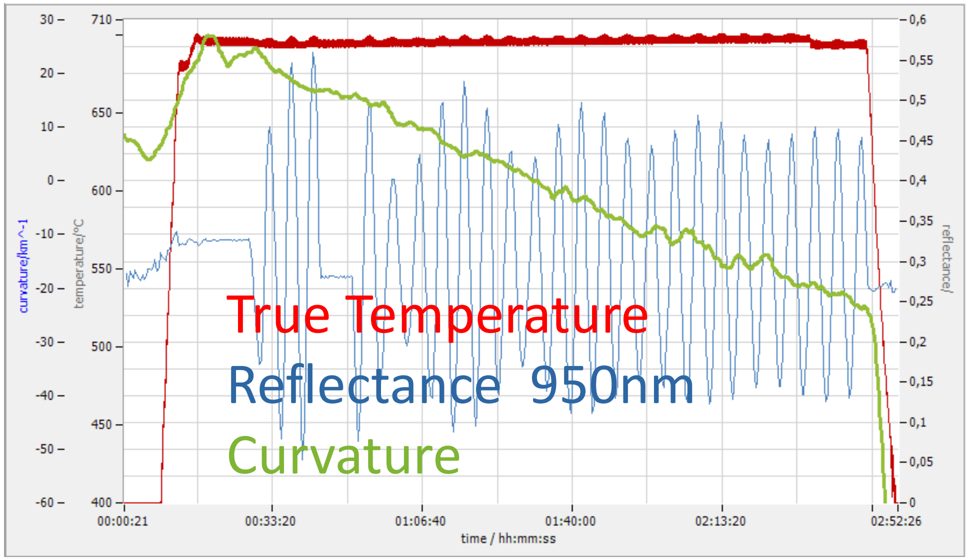
→ **latest version of AIXTRON's Aixact MOCVD software**

→ **feed forward of recipe update (new settings) for remaining 22 periods**

To be taken into account for feed-forward recipe update: the tiny but reproducible change in GRs (measured in-situ by advanved algorithms) during DBR growth

# Why growth rate is slightly changing during DBR?

DBR: 25 periods AlAs/GaAs




- Wafer is bowing during DBR growth (compressive strain in AlAs/GaAs stack)
- Thermal emission of wafer is reduced (growing DBR is covering GaAs band-edge wavelength) → reduced cooling by radiation → wafer temperature is increasing by 4K → AIXTRON's AFF technology needed
- Other effects …



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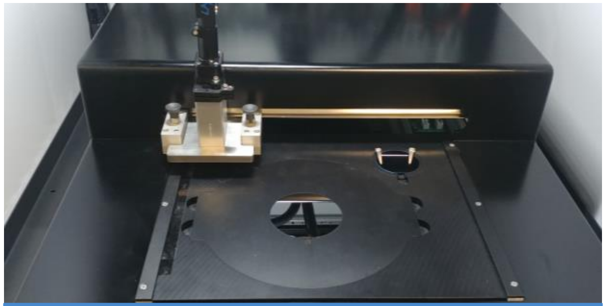
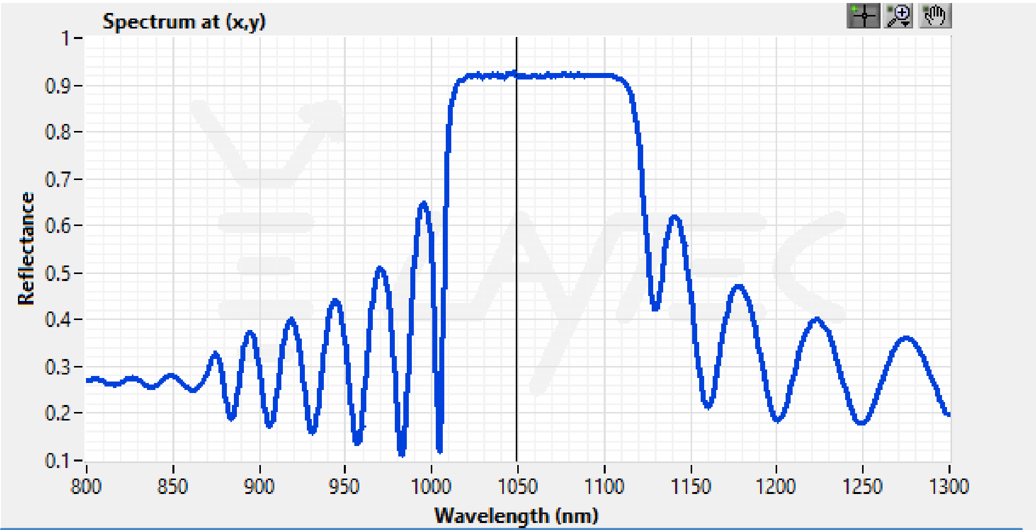
# Verification if in-situ results by ex-situ mapping


LayTec EPIX system



Mapping stage, 3“ sample holder plate

Mapping station EPIX combines white light reflectance and PL (multi-head mapping)




SESAM DBR, center of wafer, white-light reflectance



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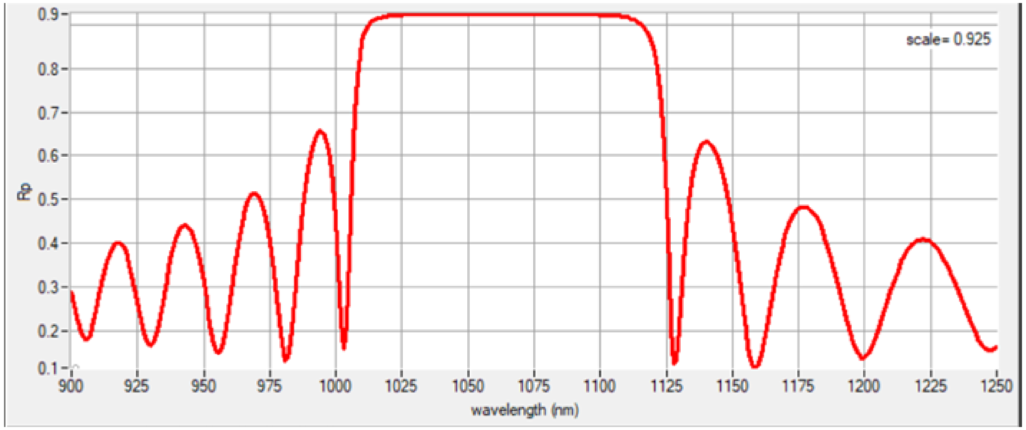
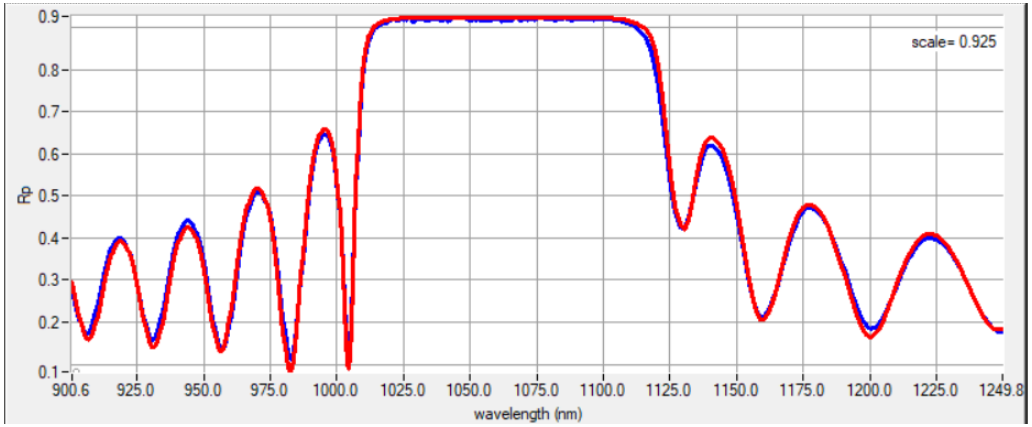
# Ex-situ growth rate (GR) analysis in center of wafer




Calculated R spectrum of ideal DBR structure (with same stop-band and side-wings as measurement) would be highly symmetric

$GR_{GaAs}$: 0,497 nm/s
$GR_{AlAs}$: 0,580 nm/s




$GR_{GaAs}$: 0,4955 nm/s → 0,4990 nm/s (+1%)
$GR_{AlAs}$: 0,5769 nm/s → 0,5839 nm/s (+1%)

*start of DBR → end of DBR*

**Measured DBR spectrum (blue) is asymmetric. Analytic model (red) derived from in-situ measured DBR growth rates → perfect agreement to measured ex-situ reflectance spectrum in center of wafer.**



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# Finally: ex-situ 2D DBR growth rate mapping


2D map of AlAs growth rate: 2% deviation center to edge

After selecting, **based on in-situ data,** the proper **DBR multi-layer model** → 2D mapping of GaAs and AlAs GRs yield highly accurate **growth rate spatial uniformity data for further optimization of the MOCVD recipe.**

**Combining in-situ analysis, 2D mapping and advanced multi-layer analyses → GR uniformity data measured even for highly complex device structures**



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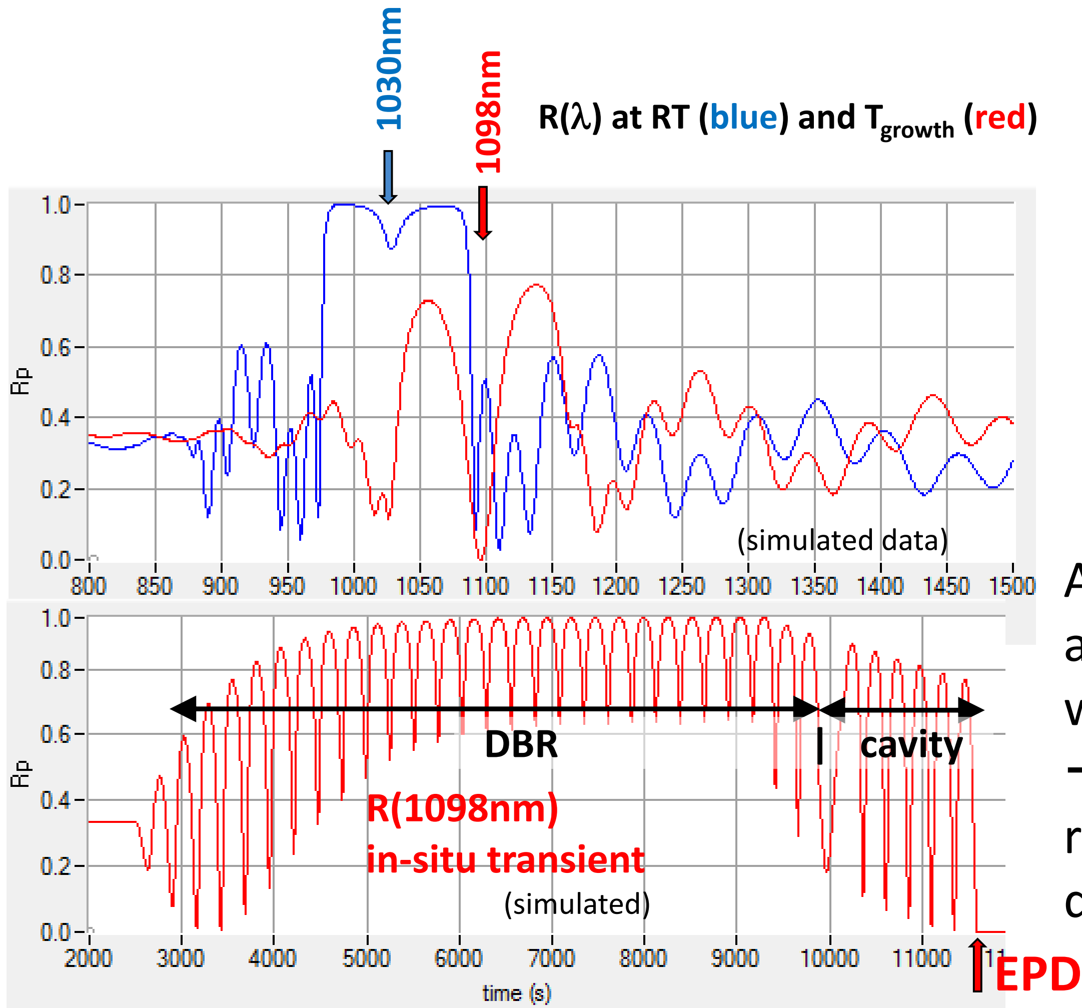
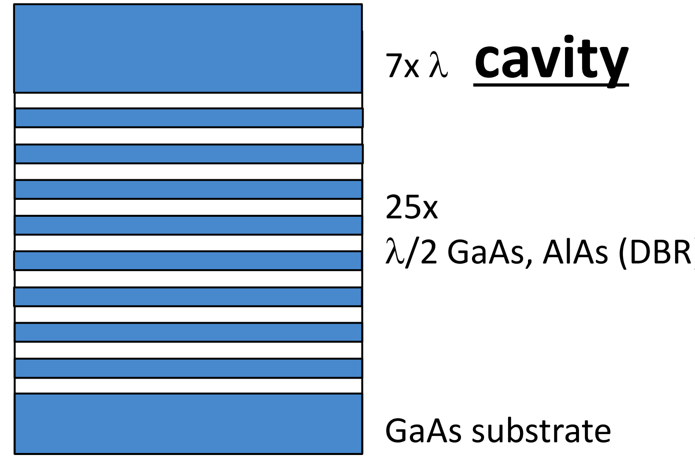
# 1030nm SESAM → cavity's end-point detection (EPD)

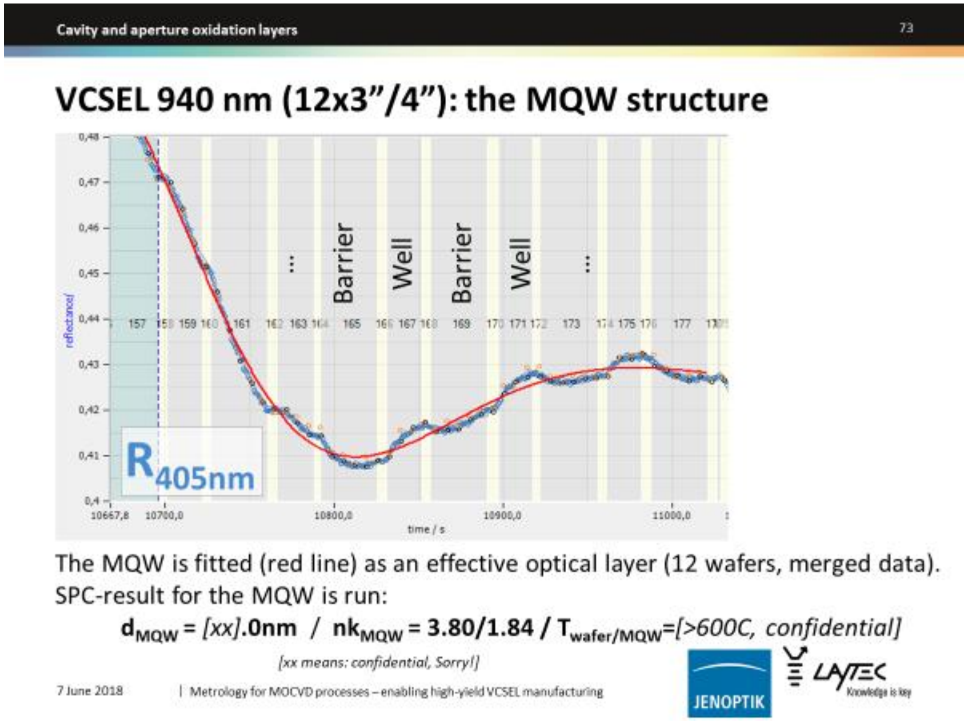



At growth temperature cavity dip and stop band are up-shifted in wavelength.
→ Select wavelength of cavity resonance at $T_{growth}$ for end-point detection (EPD) of cavity thickness!

**Spectral sensing → free choice of best wavelength for end-point detection (EPD).**
**±1nm accuracy in cavity dip – only by EPD!**

# VCSEL cavity – more detailed analysis of MQW signature




Full load (12x4") in planetary reactor. The 405nm reflectance traces of all 12 wafer-centers have been merged into a single data line.

At ICMOVPE 2018 (Nara, Japan) we already presented: the total thickness and effective nk of the MQW structure can be determined from analysis of 405nm in-situ reflectance.



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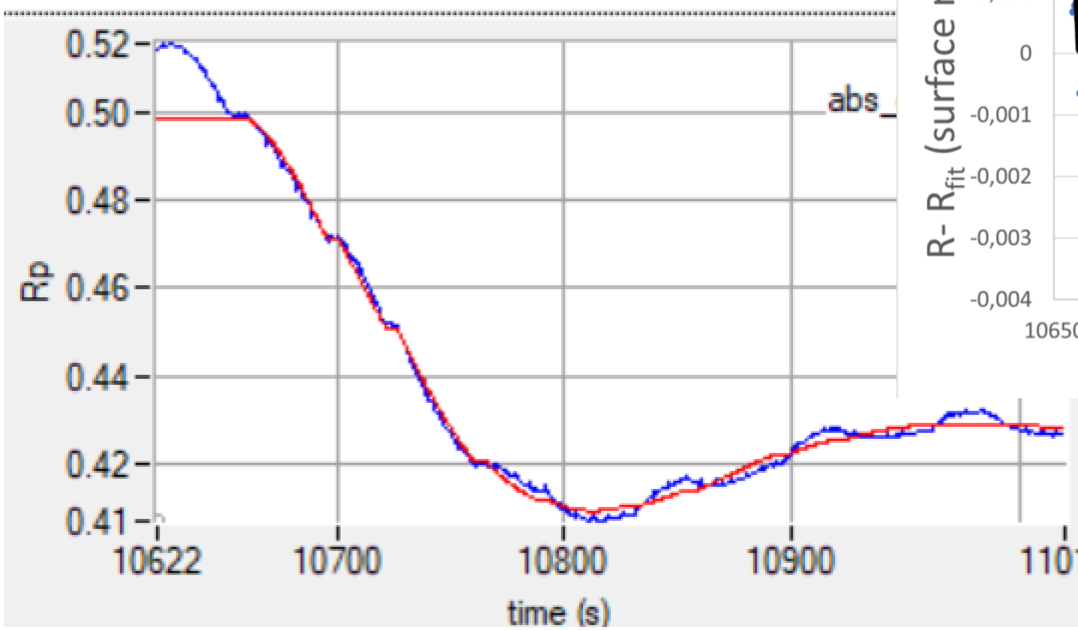
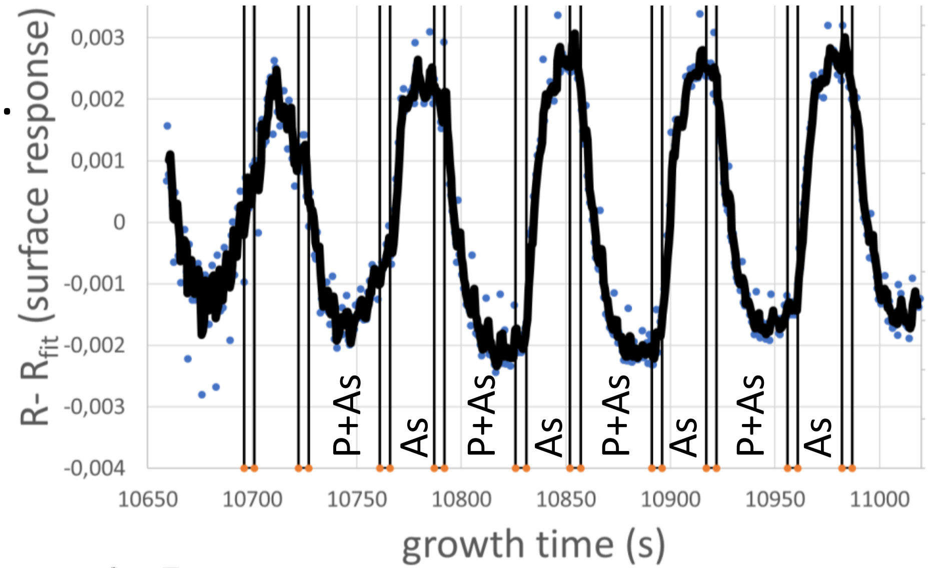
# VCSEL cavity – more detailed analysis of MQW signature

Now: closer look to the difference between R405nm fit and measurement.




Improved fit (red) to measured 405nm-reflectance (blue) of the **strained InGaAs/GaAsP MQW**. A single MQW effective nk is used. The 5s purging pauses and slightly different growth rates for barrier and well are taken into account.




The difference R-$R_{fit}$ between fit (2D growth of InGaAs wells embedded into 6 GaAsP barriers ) and measurement can not be explained by any realistic assumption regarding growth rates and nk optical properties. **CONCLUSION: THIS IS SURFACE OPTICAL RESPONSE!**



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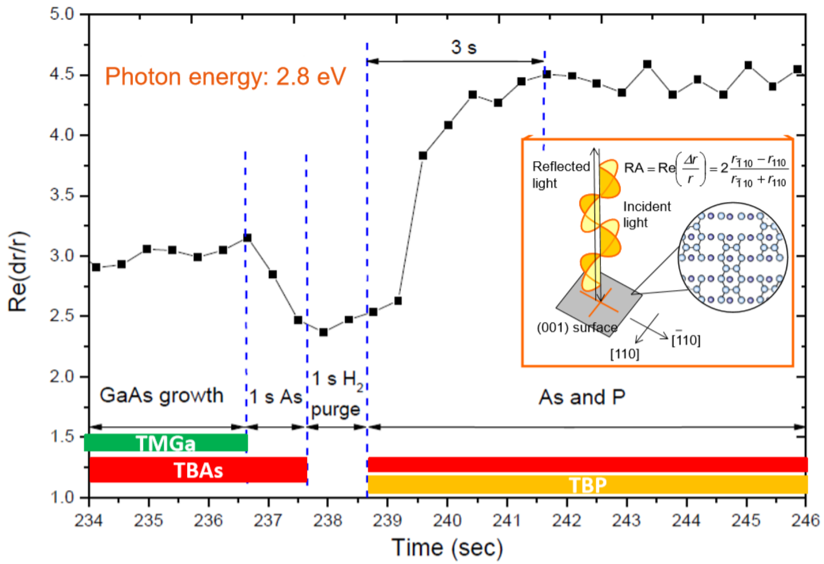
# GaAsP/InGaAs strained MQWs – former work

*In situ* RAS measurement of As/P exchange




- Stabilization of surface P content takes 3 sec at 610°C.

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Slide of Masakazu Sugiyama (University of Tokyo) as presented at LayTec Seminar 2011: RAS at 2.8eV (443nm) verifies a significant surface dimer response during GaAsP/InGaAs MQW growth for advanced photovoltaic devices.

Kobayashi et al. [1] demonstrated that RAS and SPA (surface photo-absorption, i.e., the isotropic reflectance response to changing surface conditions) both root back to the same origin: the surface reconstruction layer on top of III-V layers in MOCVD.

**InGaAs/GaAsP MQWs in 940nm VCSELs: sensing the remaining difference between R405nm reflectance and the best fit of 2D multilayer growth gives access to SPA of surface conditions during nano-structure formation in multiwafer VCSEL production MOCVD ➔ variations in barrier or well composition or thickness are expected to show up.**

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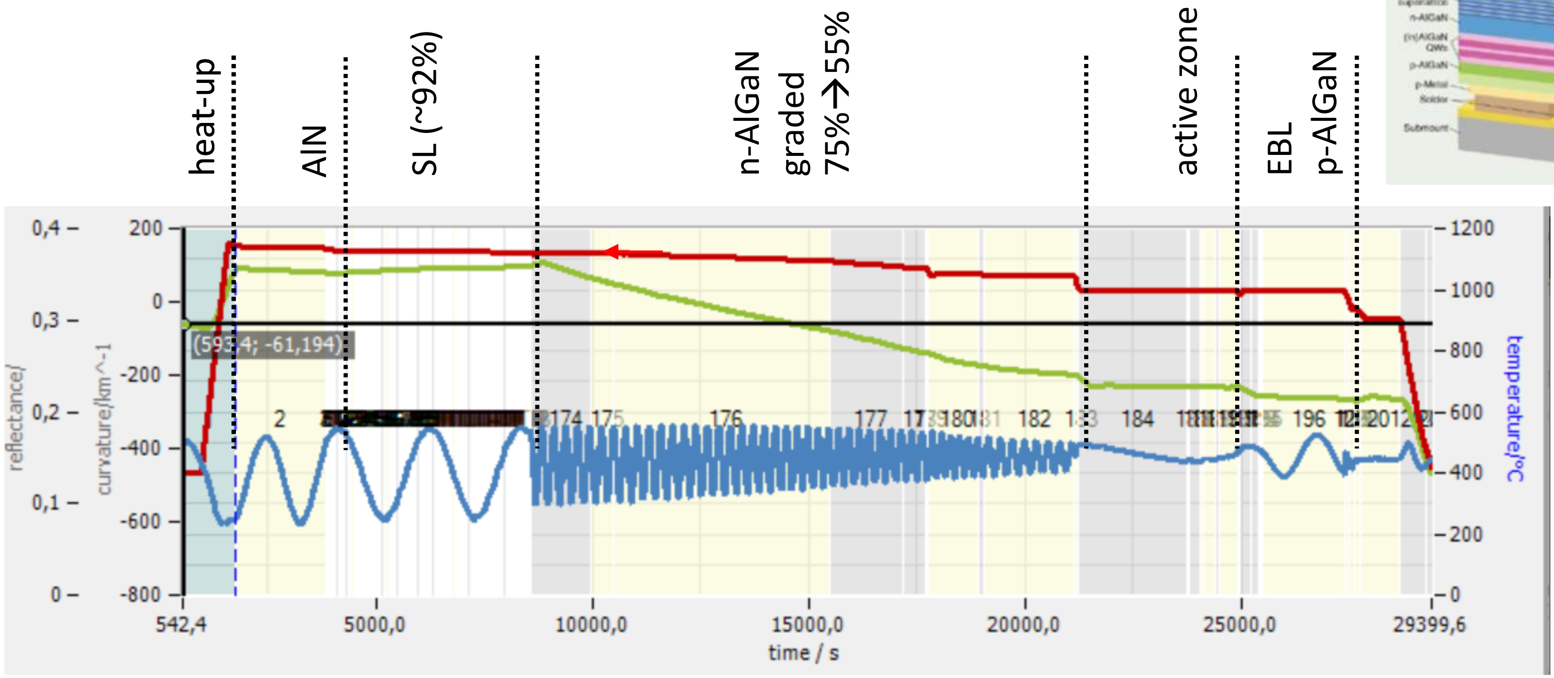
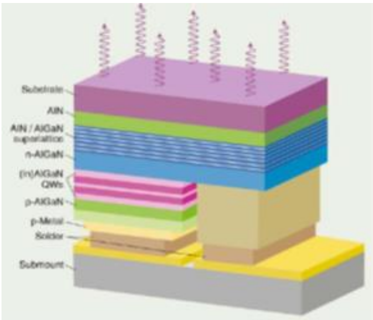
# UV-LED, 8h of Epi on Sapphire/AlN template



**Low growth rate for smoother interfaces and growth surface. Total thickness: 1.5µm AlN** (template, grown in AIXTRON G3) **+ 5-6µm of complex LED structure** (grown in 6x2“ CCS) **→ 4-wavelength (280/405/633/950nm) reflectance for providing access to all layer thicknesses.**



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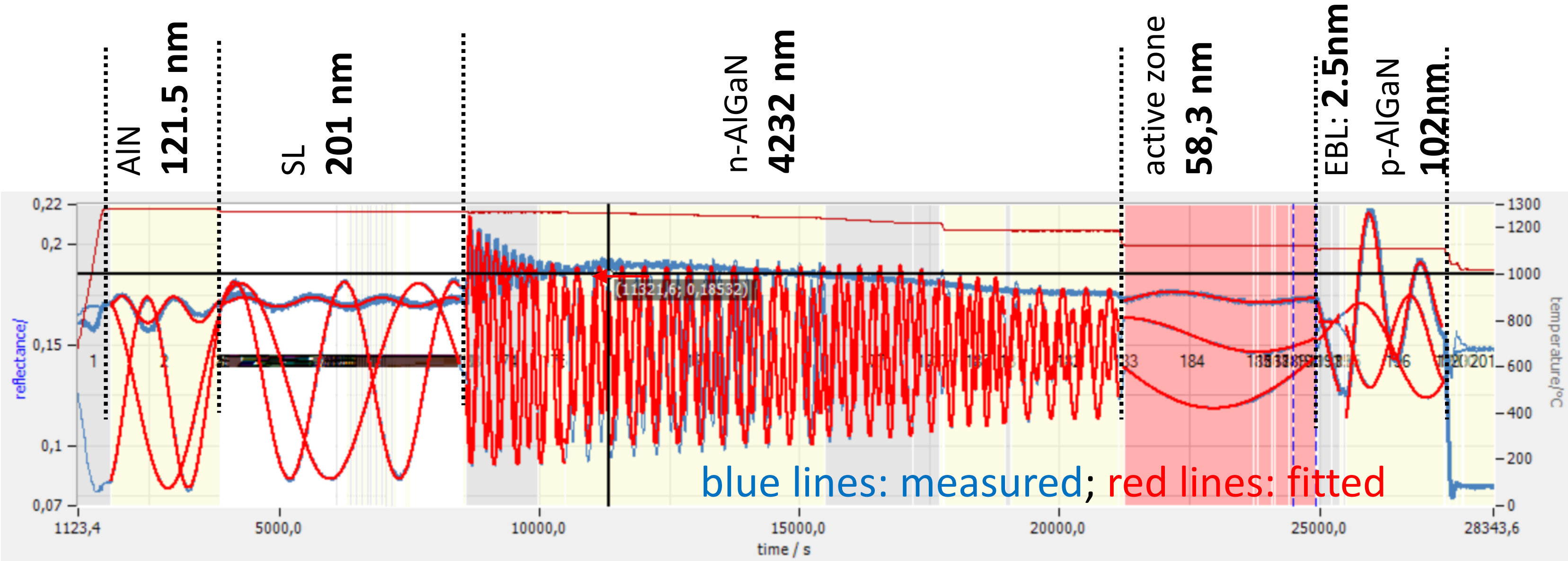
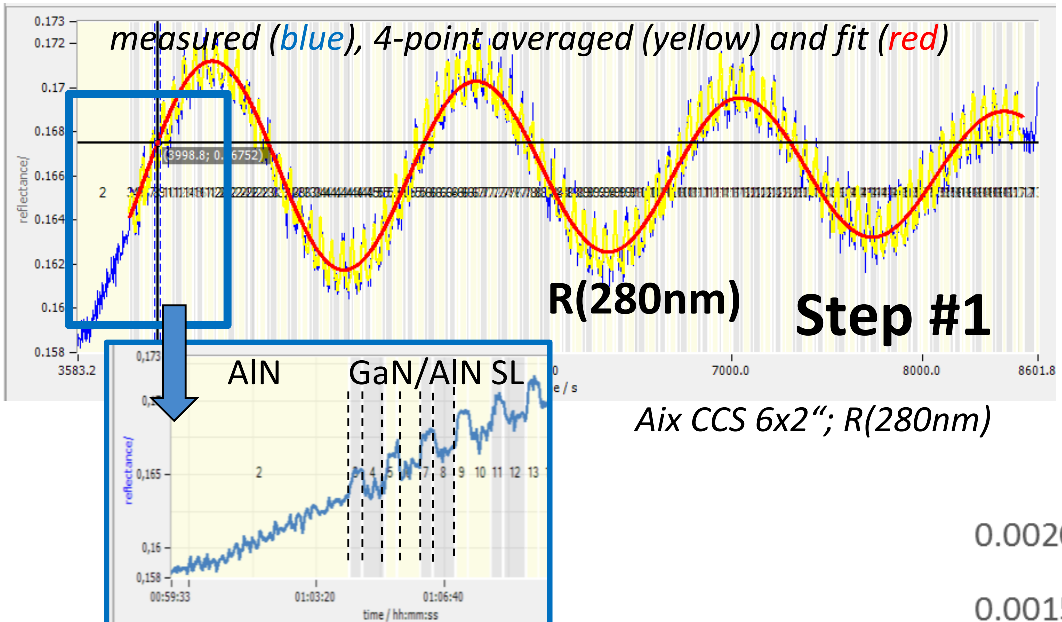
# Three wavelength growth rate analysis of UV LED




*Aix CCS 6x2"; measured reflectance 280/405/633nm (blue) and result of 3-λ-growthrate-fit (red)*

Combining reflection in UV(280nm) with near-UV(405nm) and vis(633nm)-reflection enables suppression of roughness- and bandwidth-artifacts and gives in-situ access to all layer thicknesses of the UV LED device.

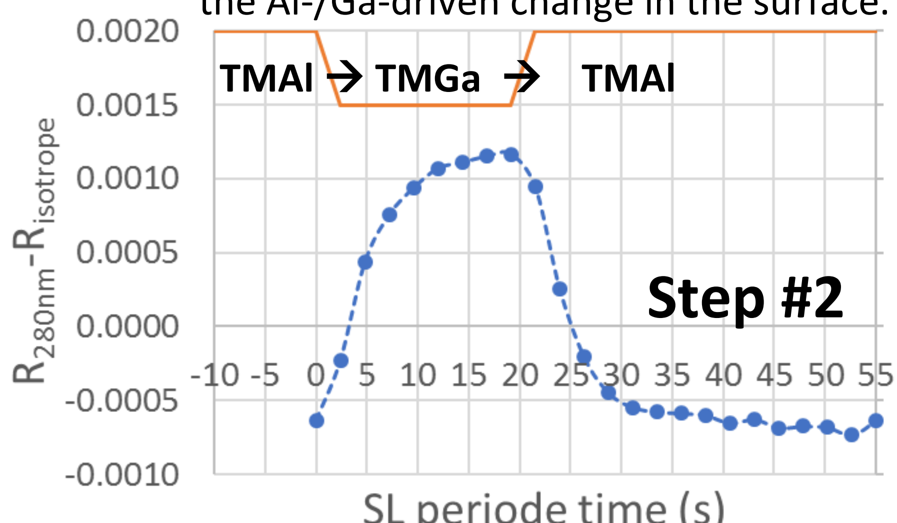
# AlN/GaN SL growth – gas phase effects to the growth surface




*Aix CCS 6x2“; R(280nm)*

← **Step #1:** fitting the 280nm reflection during initial SL growth with model “effective AlGaN layer” yields: SL total layer thickness of 201nm and the related fitted FPO reflectance trace (red line)

**Step #2:** averaging the difference (fit-measurement) over the 85 SL cycles → 280nm SPA-signal (noise of ΔR/R <5E-5) for the Al-/Ga-driven change in the surface.




**Monitoring a 85 period GaN/AlN SL for UV-LEDs by 280nm reflectance can be analyzed as a SPA experiment sensing the surface reconstruction changes from**

**Al-rich → Ga-rich → Al-rich → …**

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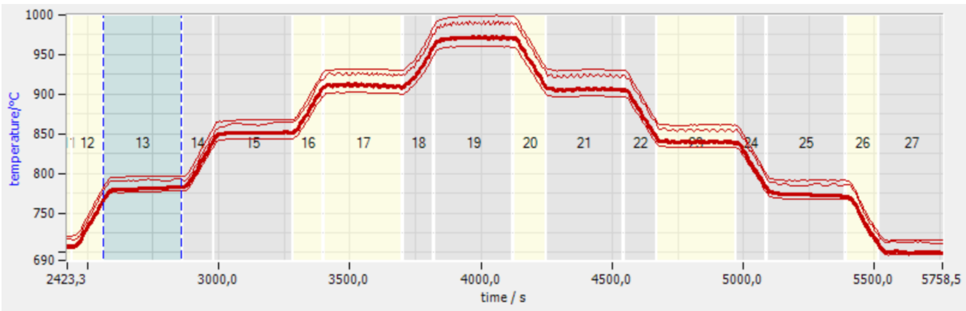
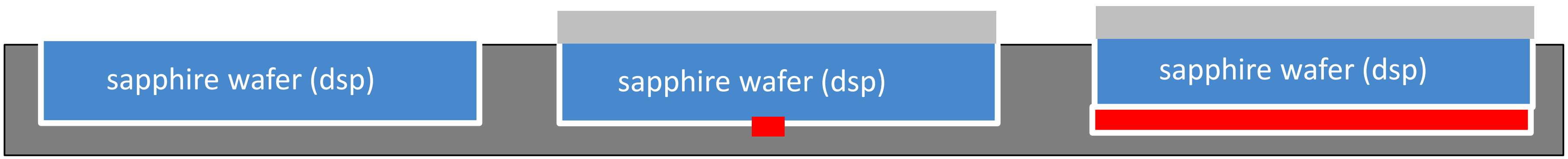
# UV LEDs – so far no in-situ access to wafer temperature




*Data: EpiCurveTT at Aixtron G3 8x2" (FBH)*

**This is work in progress.**
We used Mo (~100nm) back-side coating for getting access to $T_{wafer}$ of AlN/sapph templates at start of UV-LED process.




**Wafer #1**
bare sapphire (dsp)
$T_{pocket}$ **= 998C**

**Wafer #6**
AlN/sapphire template
Mo marker (center back-side)
$T_{wafer}$ **= 985C**

**Wafer #4**
AlN/sapphire template
Mo back-side coated
$T_{wafer}$ **= 996C**

**The AlN template wafer temperature at begin of UV-LED process is 13K below pocket (graphite/SiC) temperature.** Full Mo coating of sapphire back-side improves the heat-transfer. This approach will be used for studying wafer temperatures during UV LED processes.



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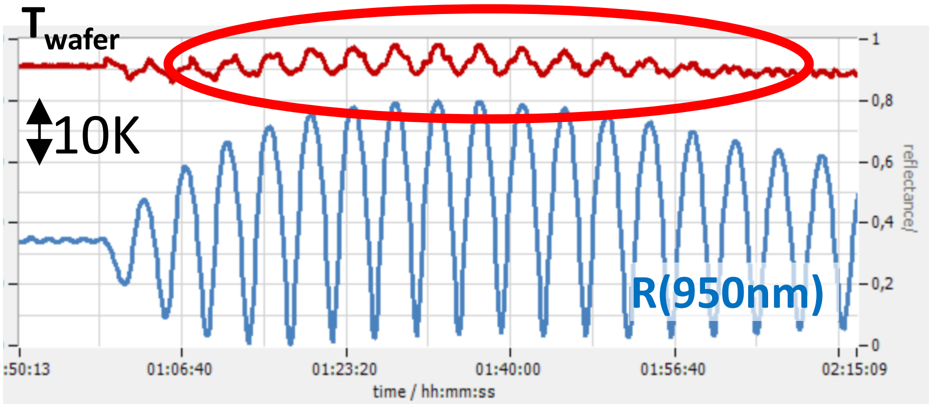
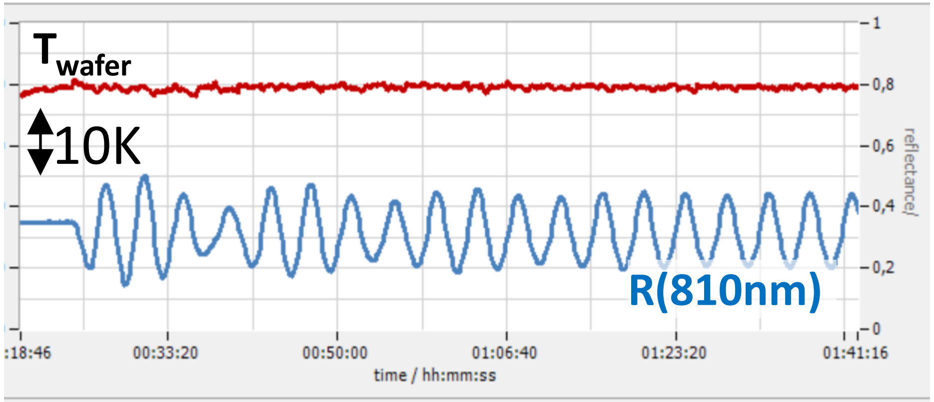
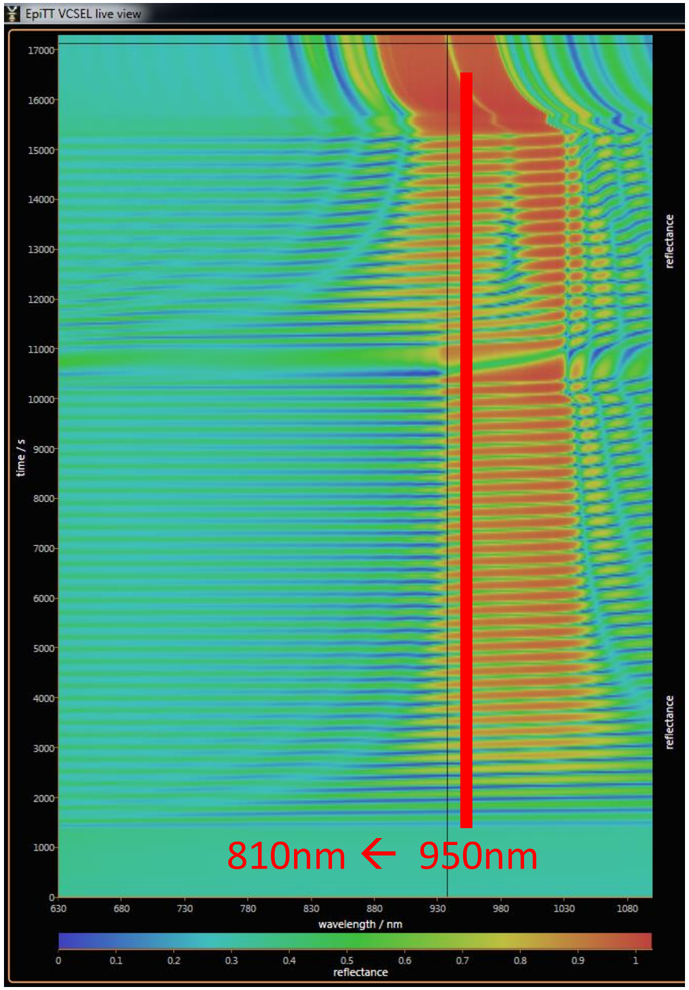
# 940nm VCSEL Run – adding a 2nd pyrometry wavelength




**950nm pyro:** wafer's thermal radiation blocked by DBR ($\varepsilon$=1-R<20%) → artifacts in $T_{wafer}$




**Second 810nm pyro:** wafer's thermal emissivity $\varepsilon$ always >60% → wafer temperature free of FPO artifacts



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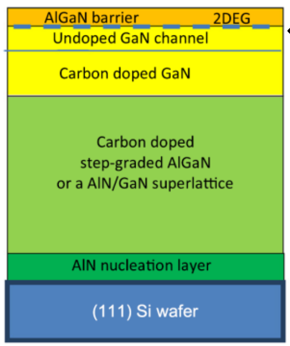
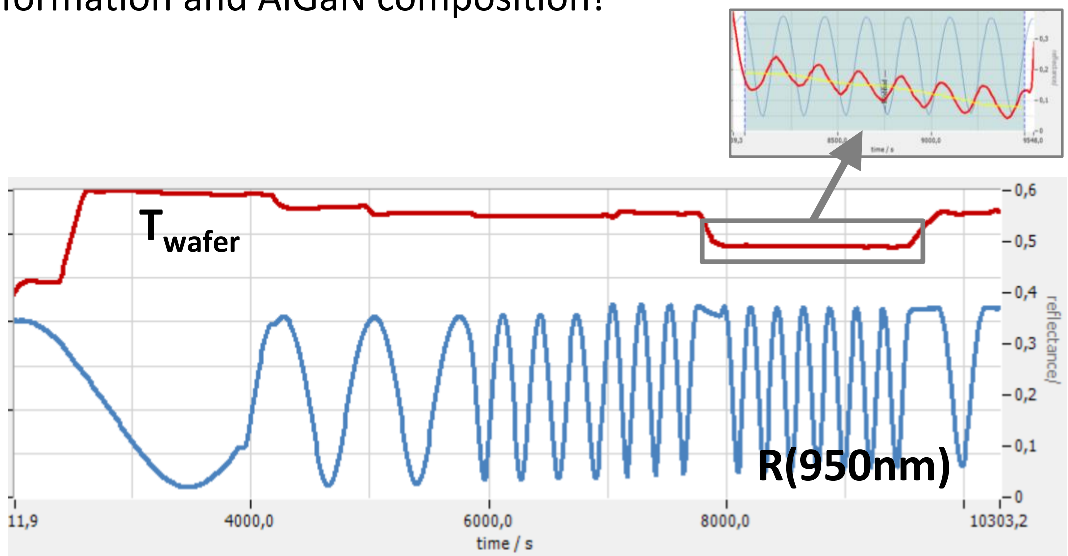
# GaN/Si HEMT – wafer temperature: ECP at its limits




**GaN/Si Power HEMT**

At the very end of epi run: accurate $TT_{wafer}$ is essential for interface formation and AlGaN composition!




Wafer temperature is measured by 950nm pyrometry, corrected for the oscillating emissivity (ε=1-R). For GaN/Si this „ε-correction“ is 35% of the signal! → We redesigned the pyrometer- and reflectometer-segments of EpiTT rigorously in order to meet the latest industries targets (±0.3K).



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# Summary & Outlook

- We have developed new methods and procedures for measuring in Aixtron's G4/G5 reactors the growth rates of thin layers in highly complex device structures.
- High-yield manufacturing of current cutting-edge devices can only be facilitated by close integration of in-situ metrology into the MOCVD tools. Epi recipe and in-situ analysis recipe communicate and send data into MES. Ex-situ mapping of Epi uniformity achieves a new level of accuracy by feeding in the results of in-situ analysis.
- Challenges in wafer temperature sensing for VCSELs and GaN/Si HEMT processes have been solved. Wafer temperature in UV LED epi is an open issue.
- Precision in in-situ reflection gives access now to surface reconstruction changes during growth.

*We acknowledge the support of German State (BmFT) within the „Advanced UV for Life“ consortium for our UV-LED projects as well as through the funding of the projects „MOCVD4.2“ and „NextLED“ both focussing on the next generation of metrology integration into advanced MOCVD systems.*



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