Connected metrology - characterizing complex layer stacks along the manufacturing chain

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MEMBER OF THE NYNOMIC GROUP

LayTec AG - a member of NYNOMIC group (an Advanced Metrology Holding)

LayTec provides: METROLOGY-based solutions to enable:

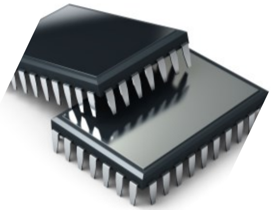
High-yield & high performance manufacturing

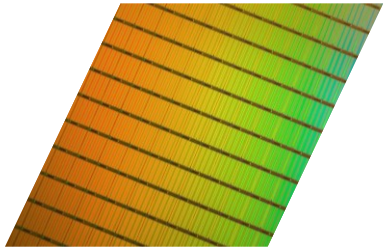
Advanced Process Control

Advanced R&D

For industry & research:

Semiconductor market





PV & large area coating

In this talk we focus on: LayTec's connected metrology for Compound Semiconductor based Power Electronics (PE)

Image credits: see last slide

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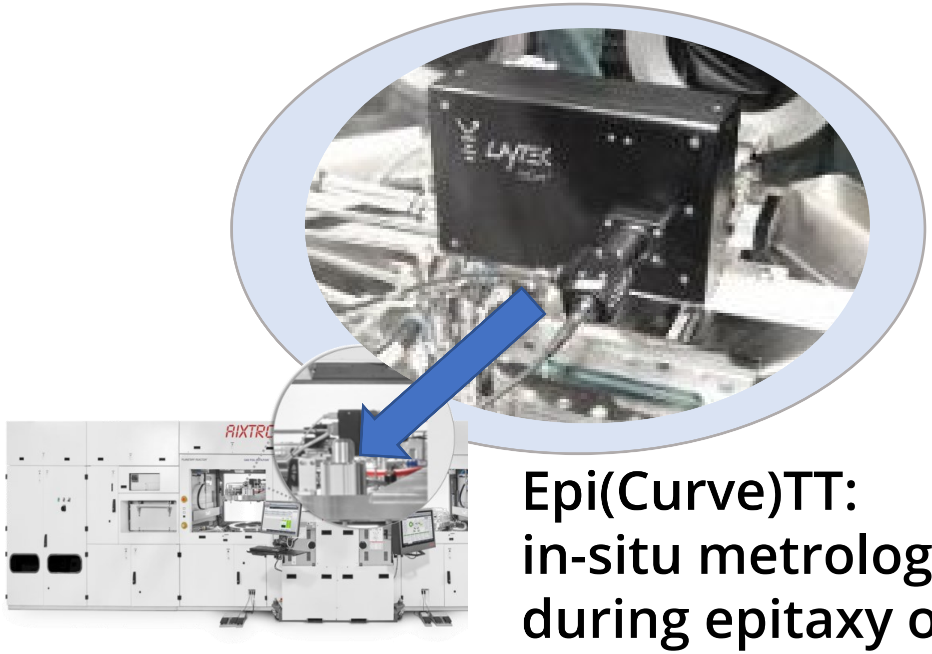
General Challenges of semiconductor industry affecting optical metrology

- **Diversification and Resilience of Global Supply Chains**
  - Fab-to-Fab process matching (Asia, Europe, North America)
- **Increasing complexity of devices**
  - increasing number of layers
  - more complex layer structures
  - tighter specifications for individual layer

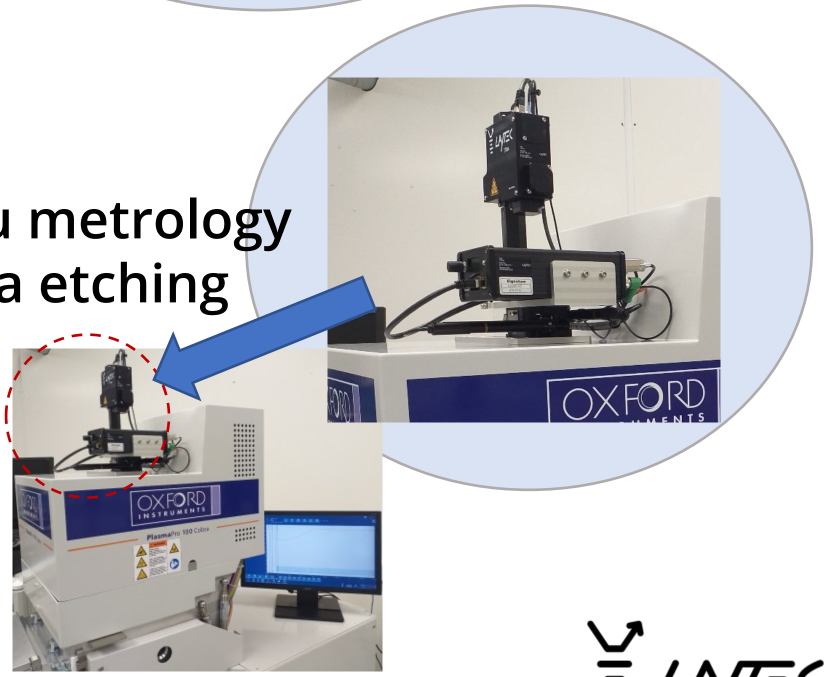
LayTec Metrology for Compound Semi PE

EpiX: optical wafer mapping



Epi(Curve)TT:
in-situ metrology during epitaxy or deposition

TRIton: in-situ metrology during plasma etching



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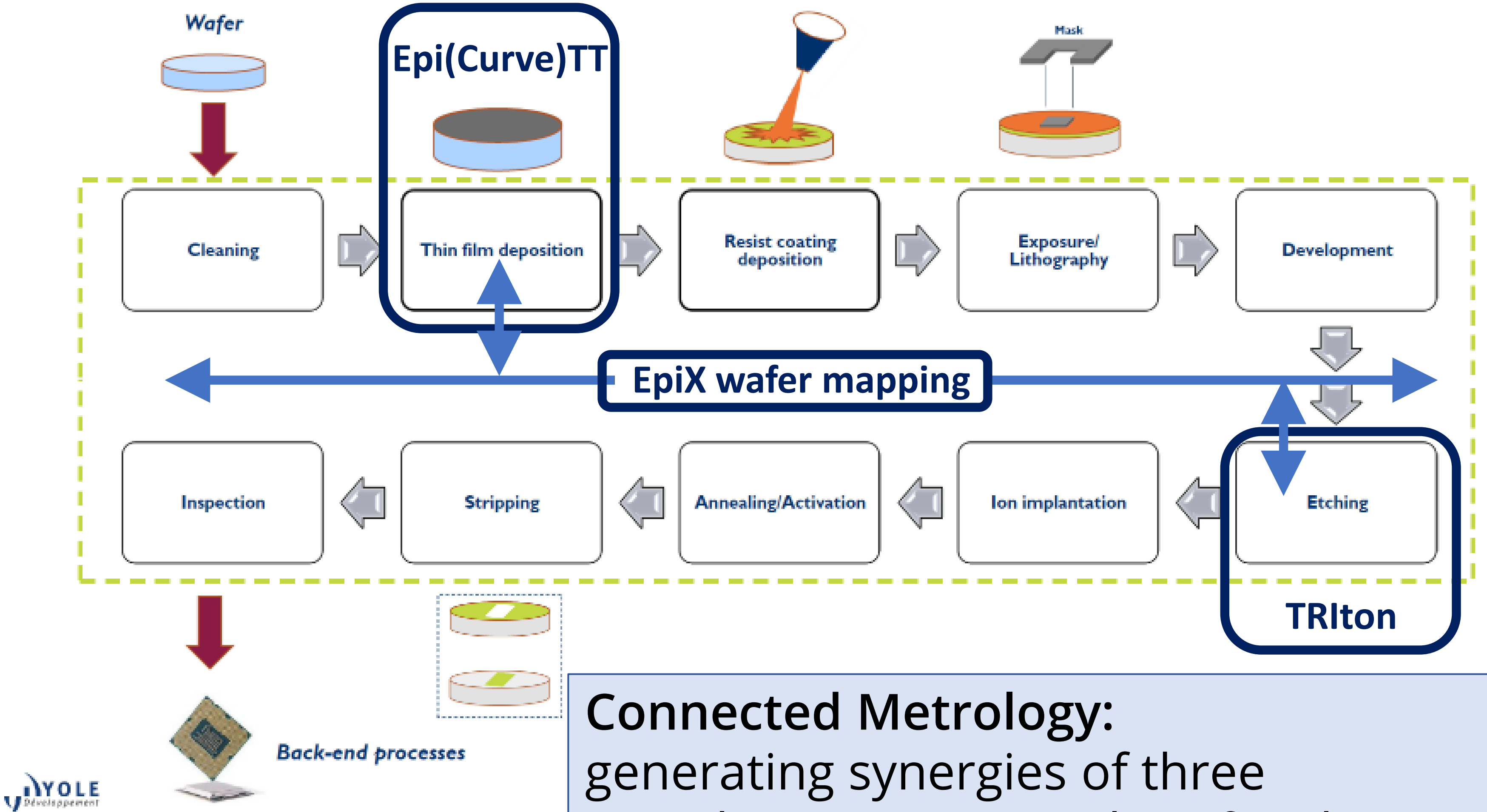
LayTec metrology - joining forces along the PE front-end processes



Connected Metrology:
generating synergies of three complementary metrology families

Connecting the data from three metrology families yields, e.g.:

- SPC of die-resolved critical process data
- Etching: blind end-point detection with nm-accuracy anywhere in the layer stack
- high-accuracy optical material data for device simulation
- …

this talk

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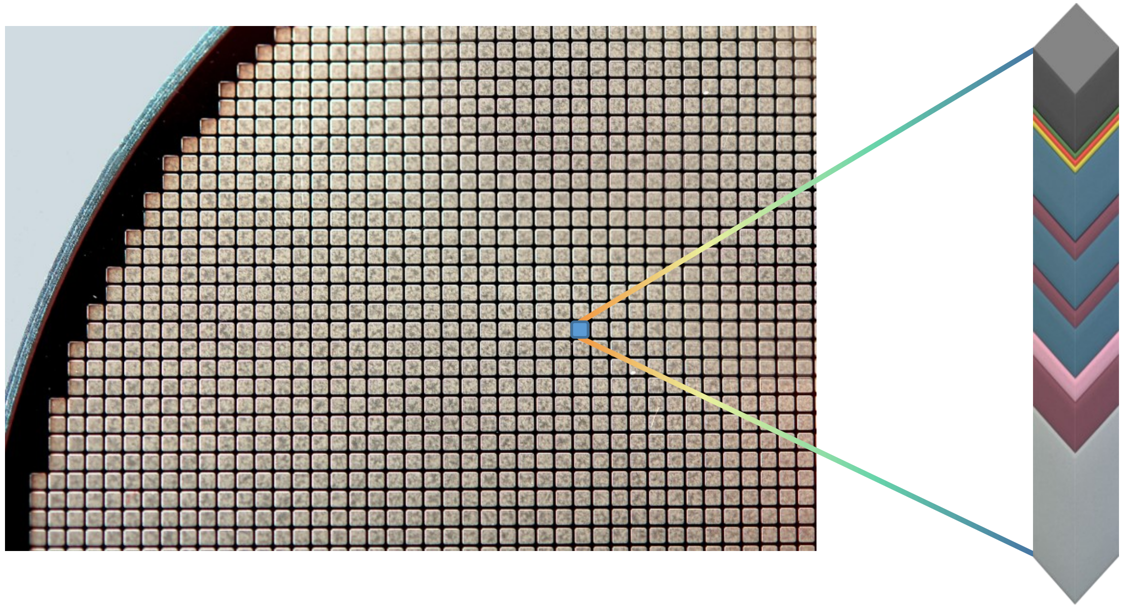
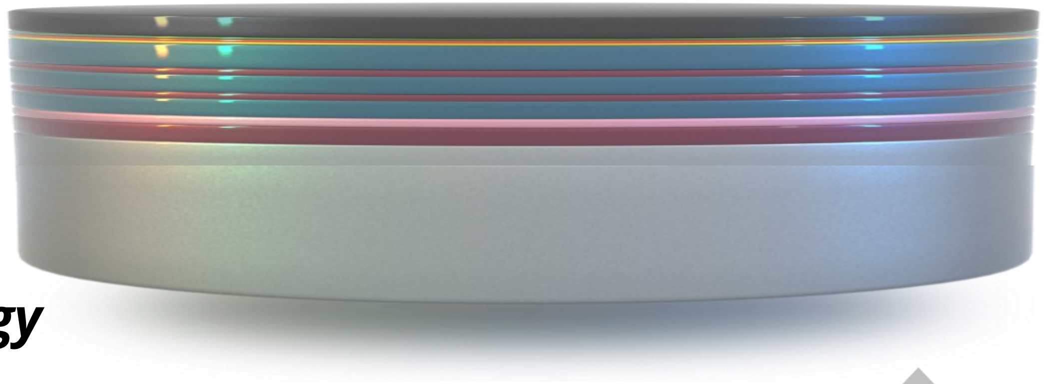
Goal of connected metrology (here: in-situ epi and 2D wafer mapping):

- Full quantification of critical layers on **die-level**
  - layer thicknesses
  - layer compositions
  - layer strain / relaxation
  - …



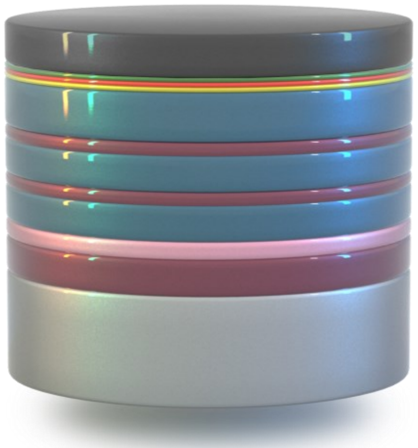
How do we get to "*Full quantification of critical layers on die-level*" ?



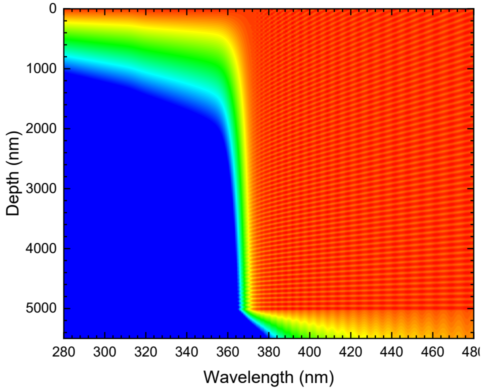
- Characterize wafer in full 3D
  by combining in-situ epi metrology
  with ex-situ 2D wafer mapping

- Transformation of full 3D wafer data into die matrix

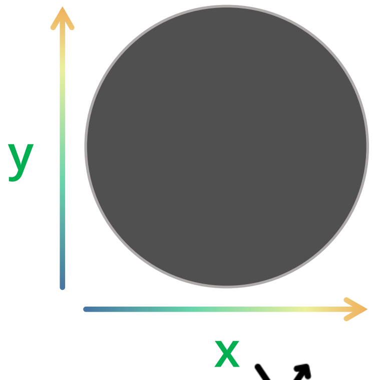
Why ex-situ optical wafer mapping with stack analysis algorithms is not sufficient for full 3D characterization?



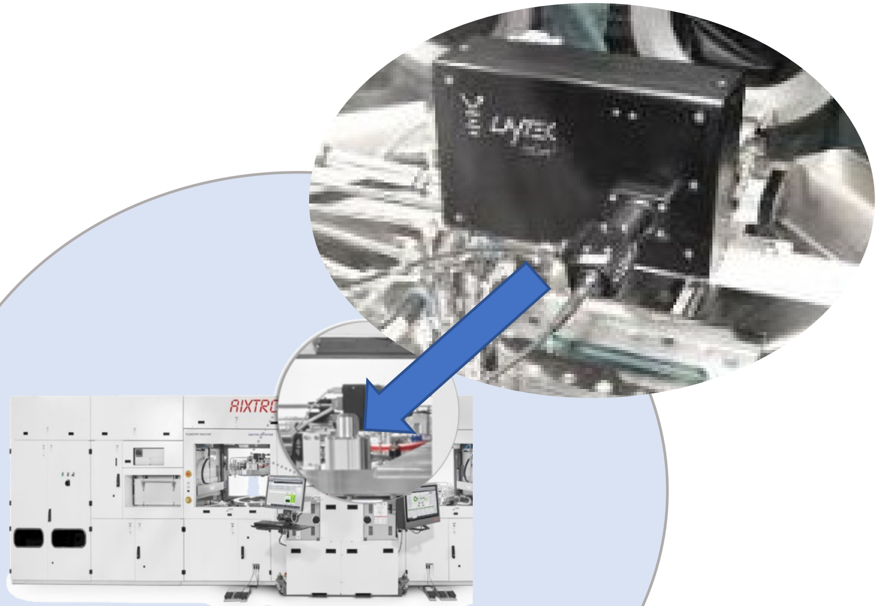
Simulated EM field
inside GaN-on-Si HEMT



- Depth information usually blocked (UV) / disturbed (vis-NIR) in ex-situ measurements of Epi-wafers
- for complex structures no nondestructive metrology can achieve full 3D characterization alone
- **Need to combine measurement results from complementary metrology tools for advanced 3D layer stack analysis**

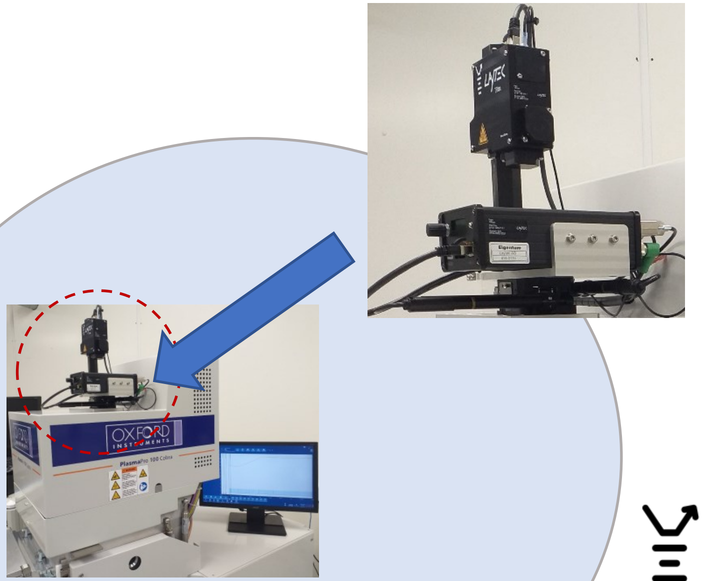


LayTec Metrology



In-situ metrology during epitaxy or deposition

Wafer mapping



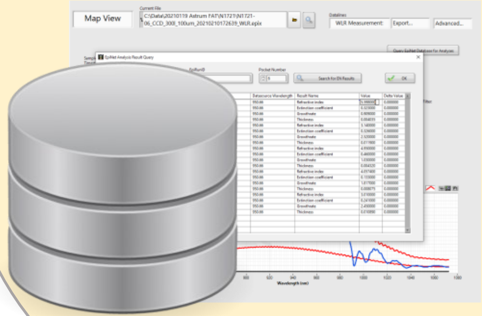
In-situ metrology during plasma etching

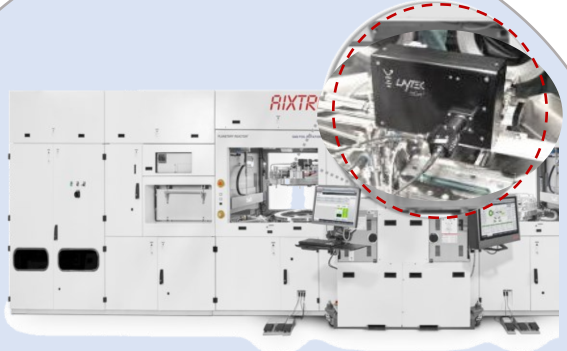
- The identical wafer is measured 3+ times

Customer MES

Wafer mapping

Database of measured data





In-situ metrology during epitaxy or deposition

In-situ metrology during plasma etching

- The identical wafer is measured 3+ times
- The amount of information increases

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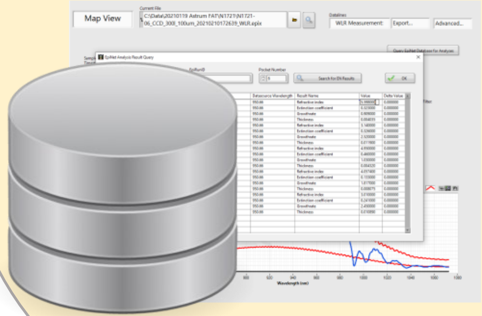
The LayTec “Metrology Ecosystem“

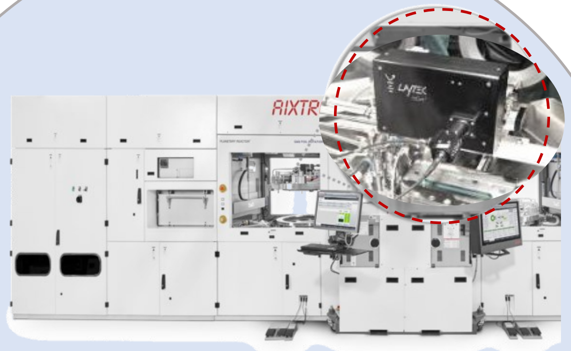
Wafer mapping

spatial variation
of layer properties

Database of measured data



in-situ measured layer thickness
and other layer properties



In-situ metrology during
epitaxy or deposition

end point detection based
on actual layer thickness

In-situ metrology during
plasma etching

- The identical wafer is measured 3+ times
- The amount of information increases and is combined for improved analysis in downstream processes

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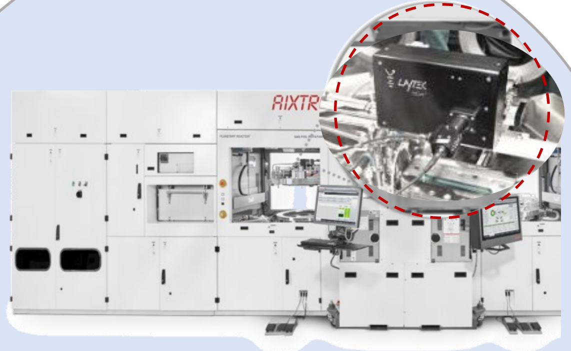
The LayTec “Metrology Ecosystem“

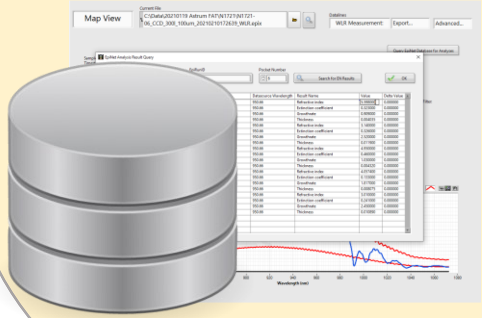
Ex-situ XRD (e.g. Panalytical) … takes advantage and provides complementary data

in-situ measured layer thickness and other layer properties



In-situ metrology during epitaxy or deposition

Database of measured data



Wafer mapping

spatial variation of layer properties

end point detection based on actual layer thickness

In-situ metrology during plasma etching

- The identical wafer is measured 3+ times
- The amount of information increases and is combined for improved analysis in downstream processes
- Team-work with XRD → access to very thin layers

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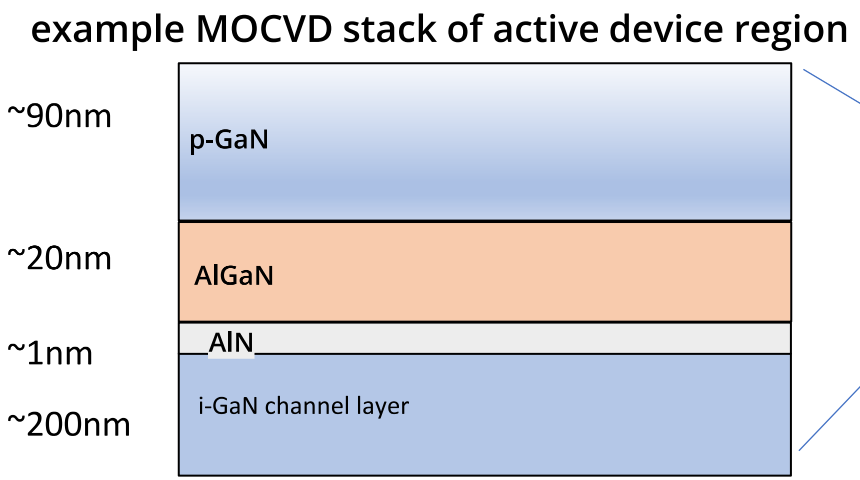
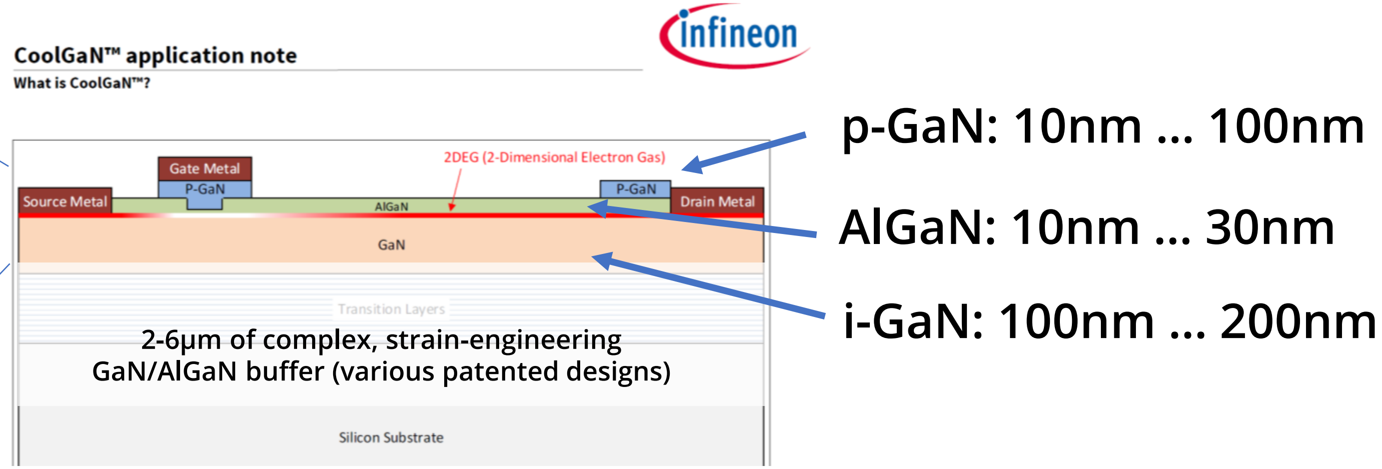
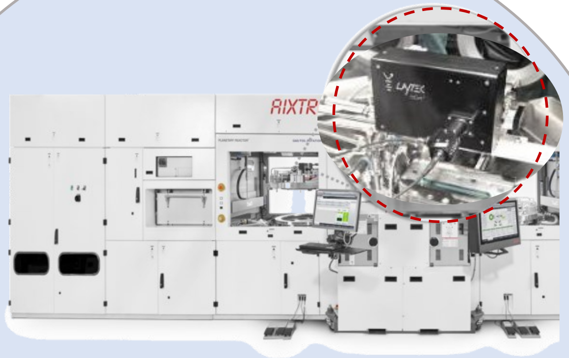
GaN/Si HEMT production – film thickness control during MOCVD AND Etching





- For cost reasons: large 200mm (soon: 300mm) silicon wafers & extreme epi and etching uniformity is required
- optical in-situ control on the level of 0.5nm (~1 atomic monolayer) is a MUST!

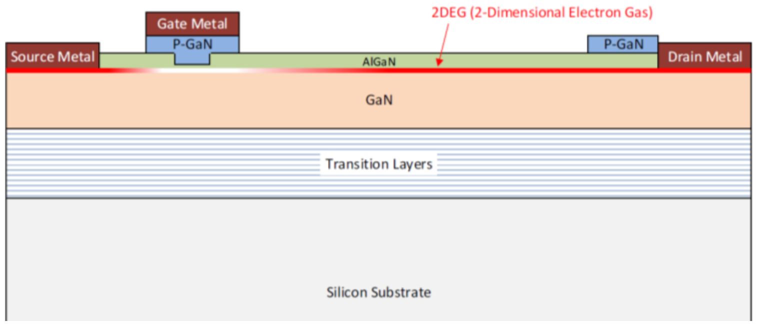
The LayTec “Metrology Ecosystem“ for GaN-on-Si HEMTs



In-situ metrology during epitaxy or deposition

Wafer mapping

In-situ metrology during plasma etching



Goal:

- die-level quantification of entire stack
- highest accuracy for critical layers (e.g., barrier)

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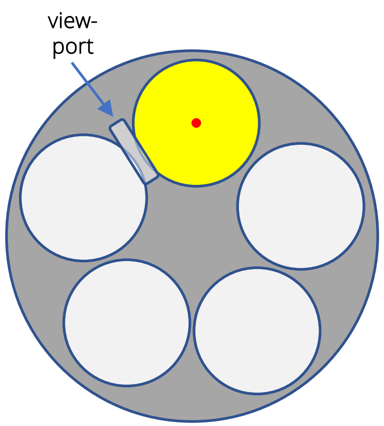
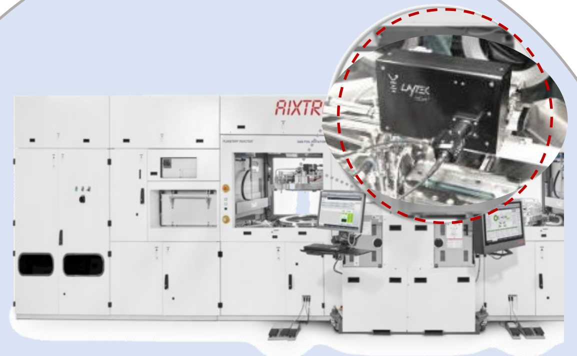
Step 1 – in-situ – 1D (z) in center of one selected wafer



Example: 5x 200mm Si,
Planetary Reactor©,
30 RPM



In-situ metrology during epitaxy or deposition

- LayTec EpiCurveTT
- every 2 s measurement of
  - temperature
  - multi-λ reflectance
  - local curvature

  at center of specific wafer
- typical growth time: few hours
- sensitivity of in-situ measurement unchanged from first to last layer

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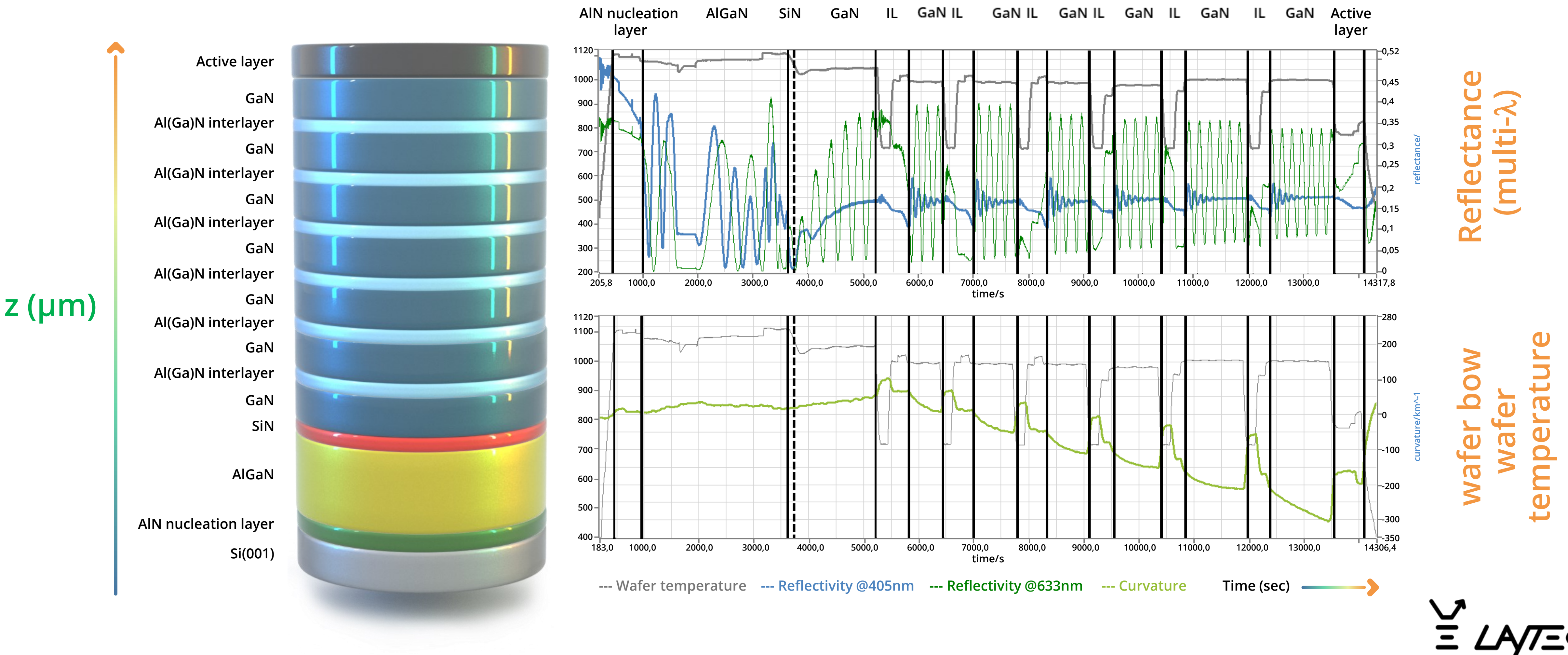
GaN-on-Si HEMT: in-situ data synchronized to epi steps



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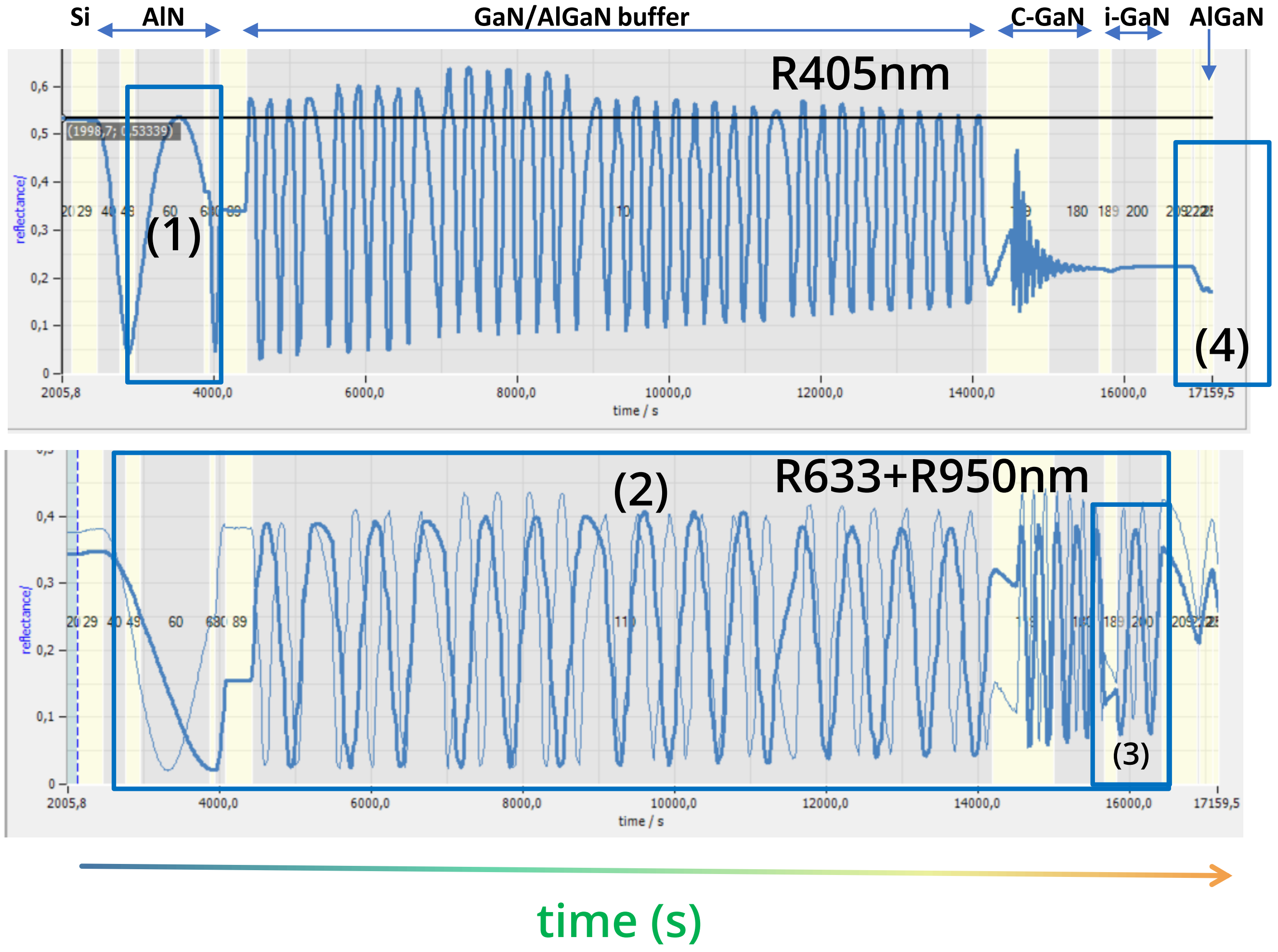
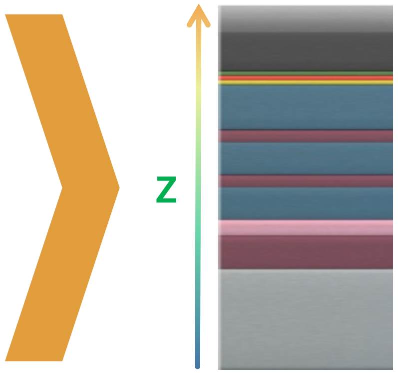
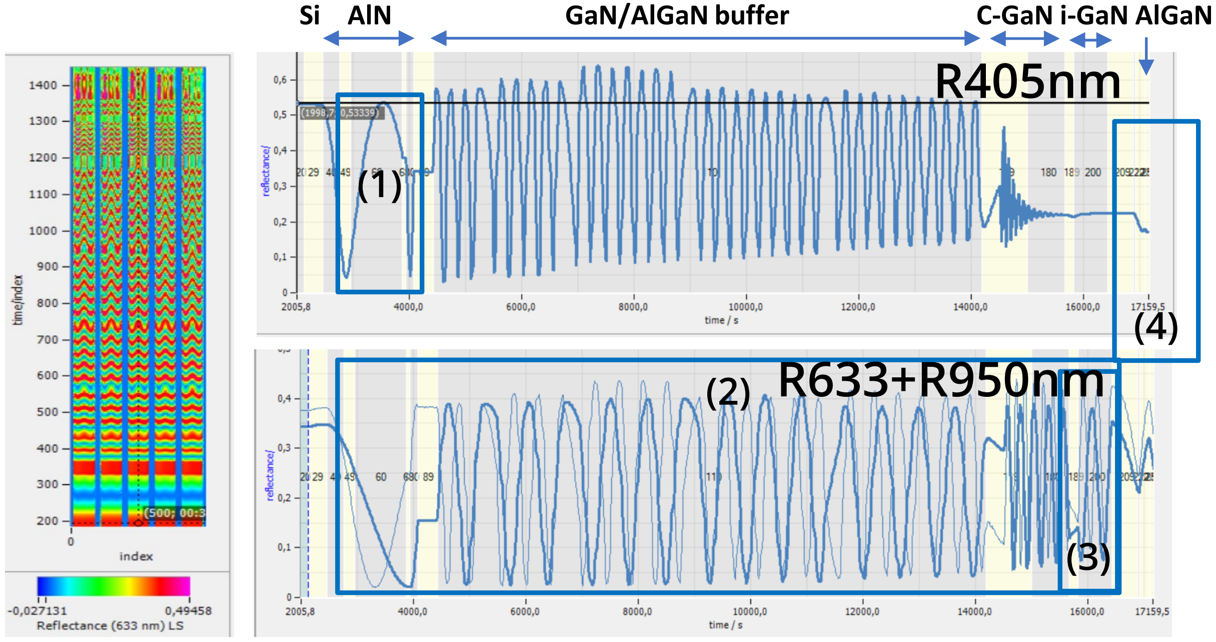
Step 1a – in-situ – 1D (z)

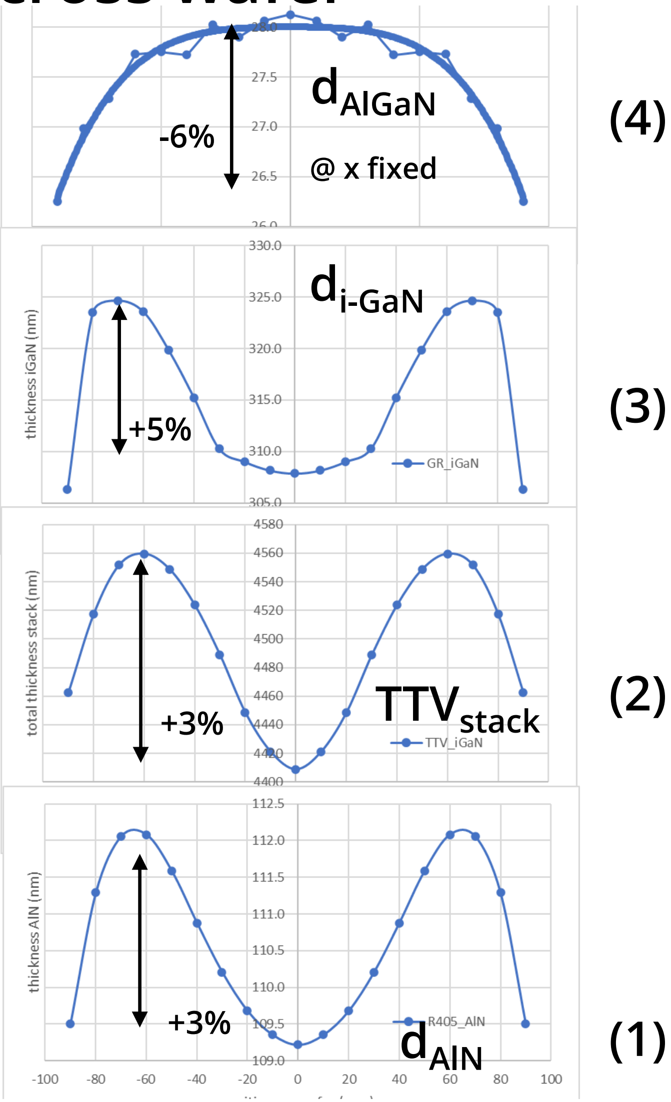




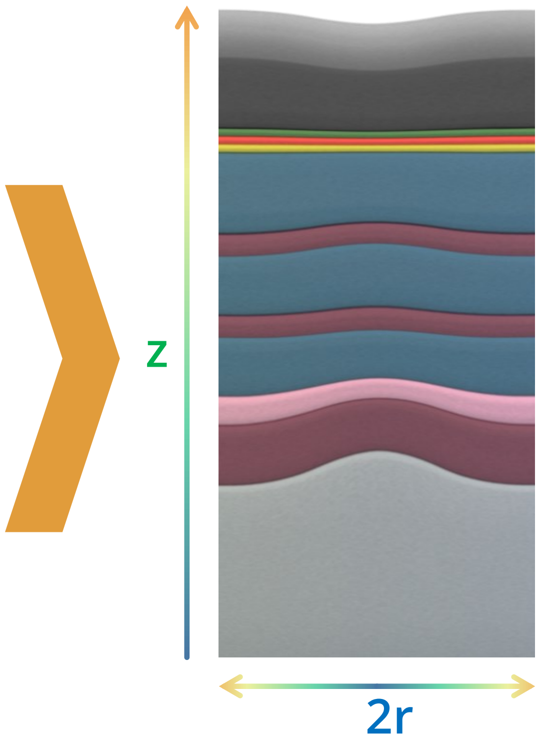
- Increasing complexity of devices requires continuous enhancements of individual measurement methods
  - shorter reflectance wavelengths to analyze thinner layers (with higher Al-content)
  - advanced analysis algorithms for multi-layer-analysis / multi-wavelength-fits / …

Step 1b – 2D (r & z), extending analysis across wafer



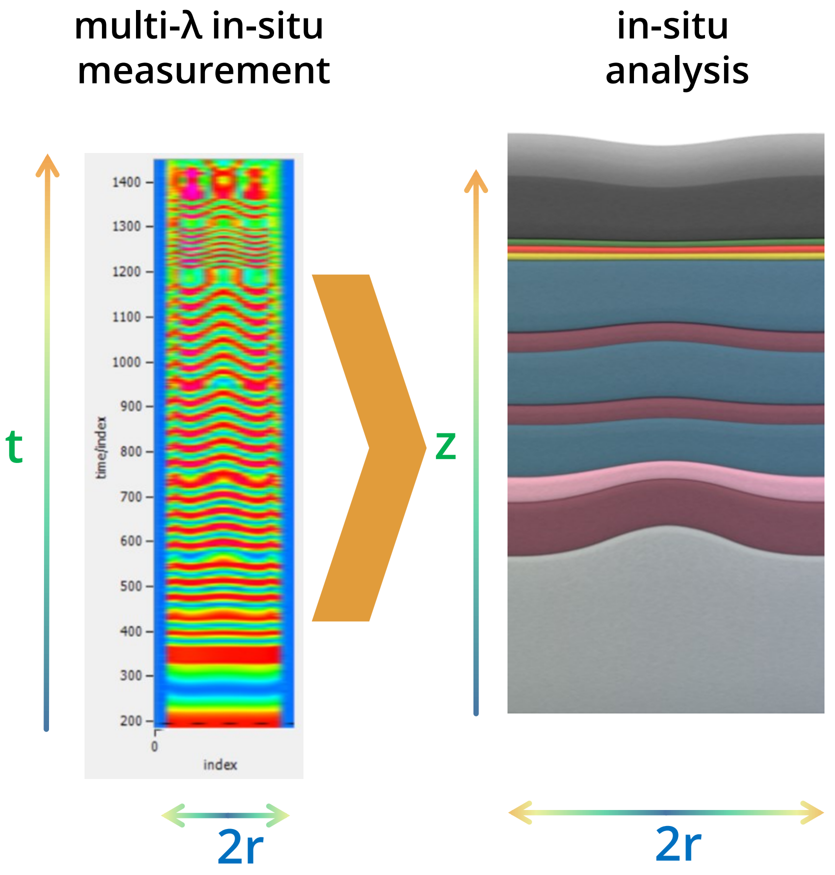


10 wafer zones → 19 radial points



- Identical analysis recipe as for wafer center gives radial distribution of individual layer parameters

Summary in-situ analysis



- Multi-λ reflectance measurement & local curvature measurement over time and radius
- Radially resolved stack information derived through analysis of in-situ measurements

Step 2 – WLR Mapping – 2D (x&y)


Wafer mapping

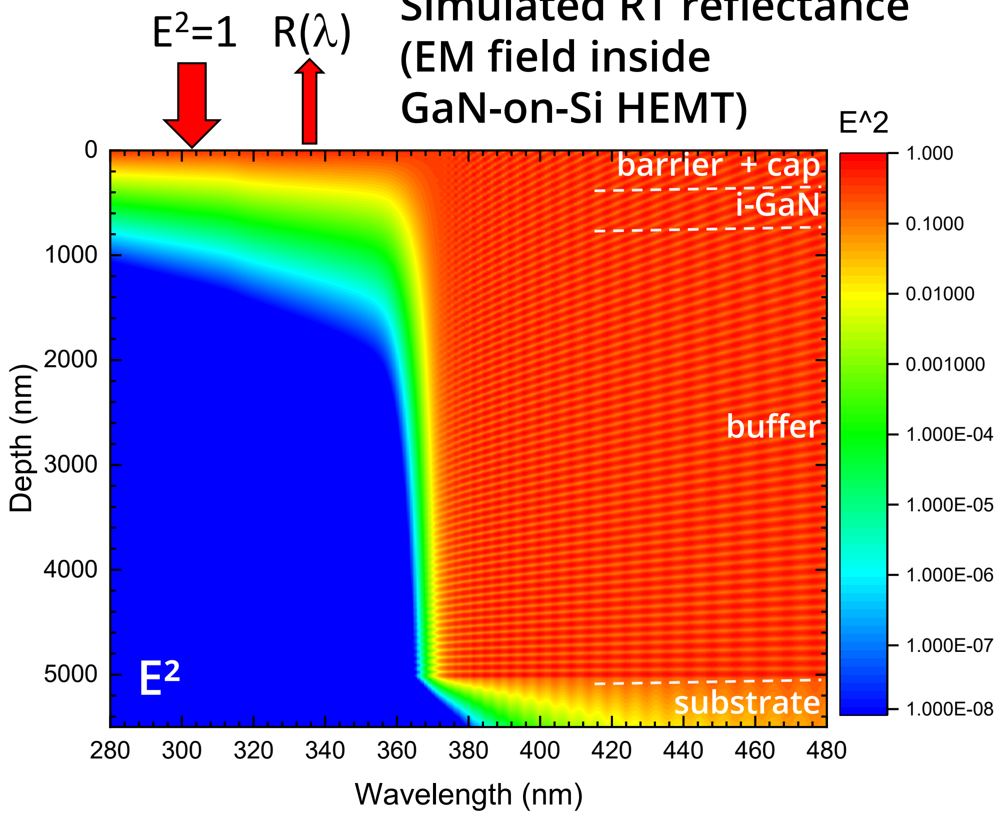
- LayTec EpiX
- White light reflectance and photoluminescence ex-situ wafer mapping
- x/y mapping @ 250-2400 nm

Goal:

- obtain x/y quantification of critical layers (e.g., barrier)
- derive die-level quantification of entire stack

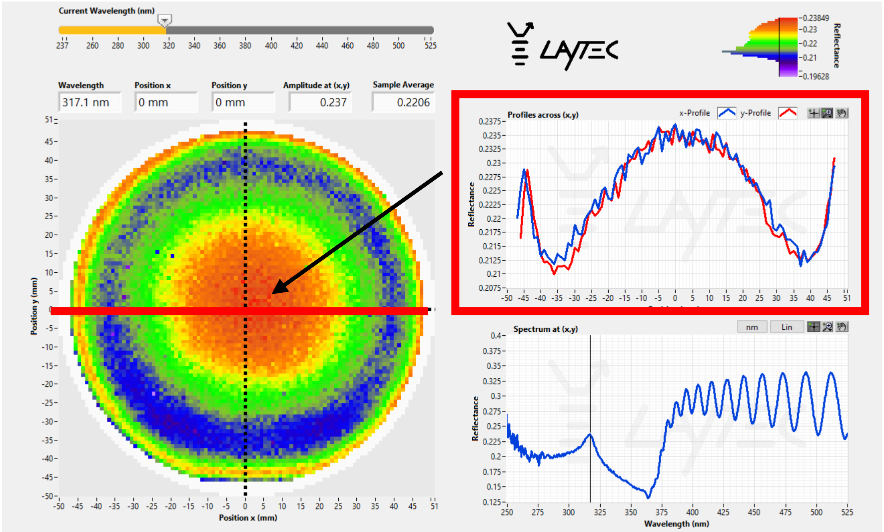
Step 2 – WLR Mapping – 2D (x&y)

Simulated RT reflectance (EM field inside GaN-on-Si HEMT)

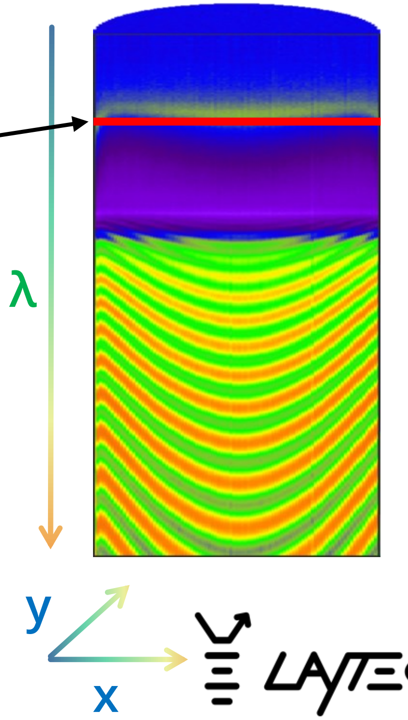


Color-Code = Lg-scale, normalized to incoming intensity of 1.0

- selection of suitable spectral region for analysis of dedicated layers
- UV → upmost few hundred nm → barrier and neighboring layers
- visible → total thickness variation → mainly buffer



Normalized measurement data view



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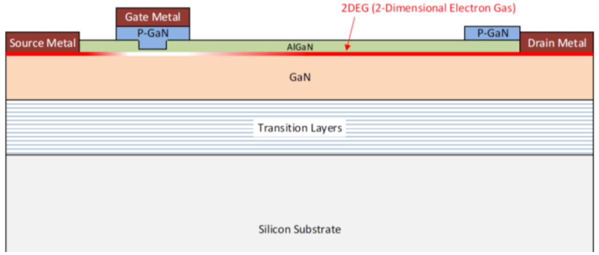
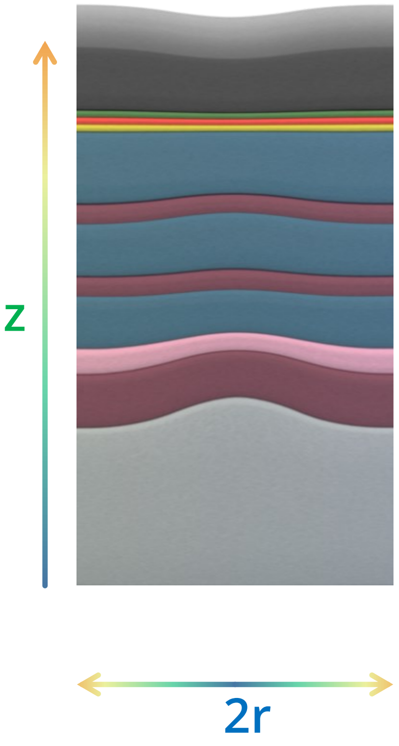
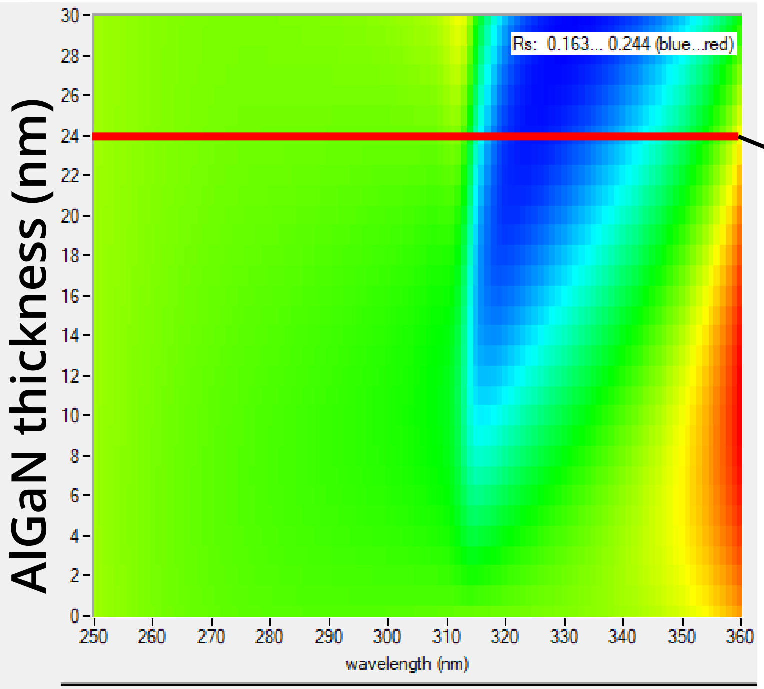
Step 2 – WLR Mapping – UV spectral fitting of HEMT structures

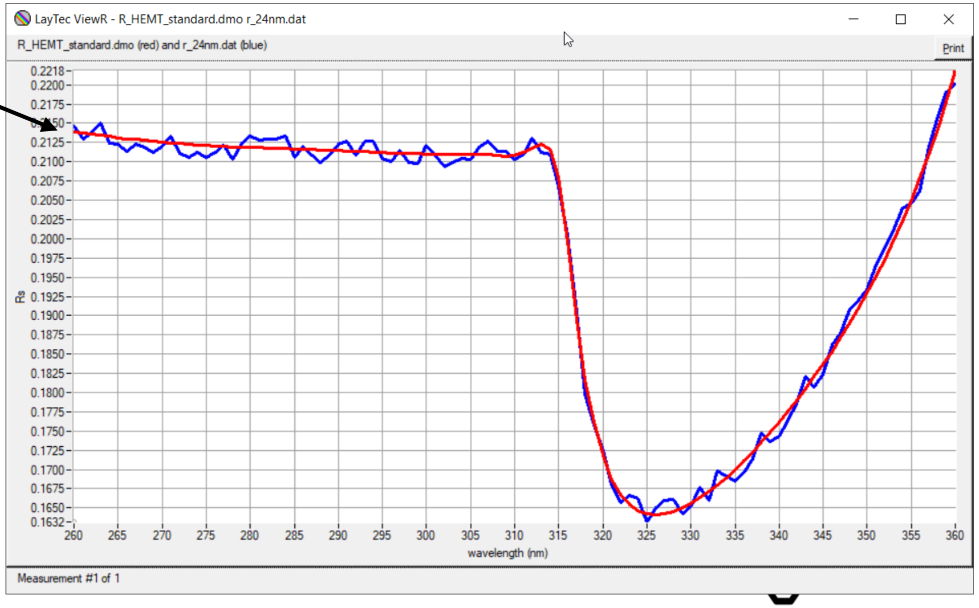


- radial profile of layer properties of entire stack available from in-situ data
- For critical layers in upmost few hundred nm derive x/y resolved layer properties from full spectral fitting

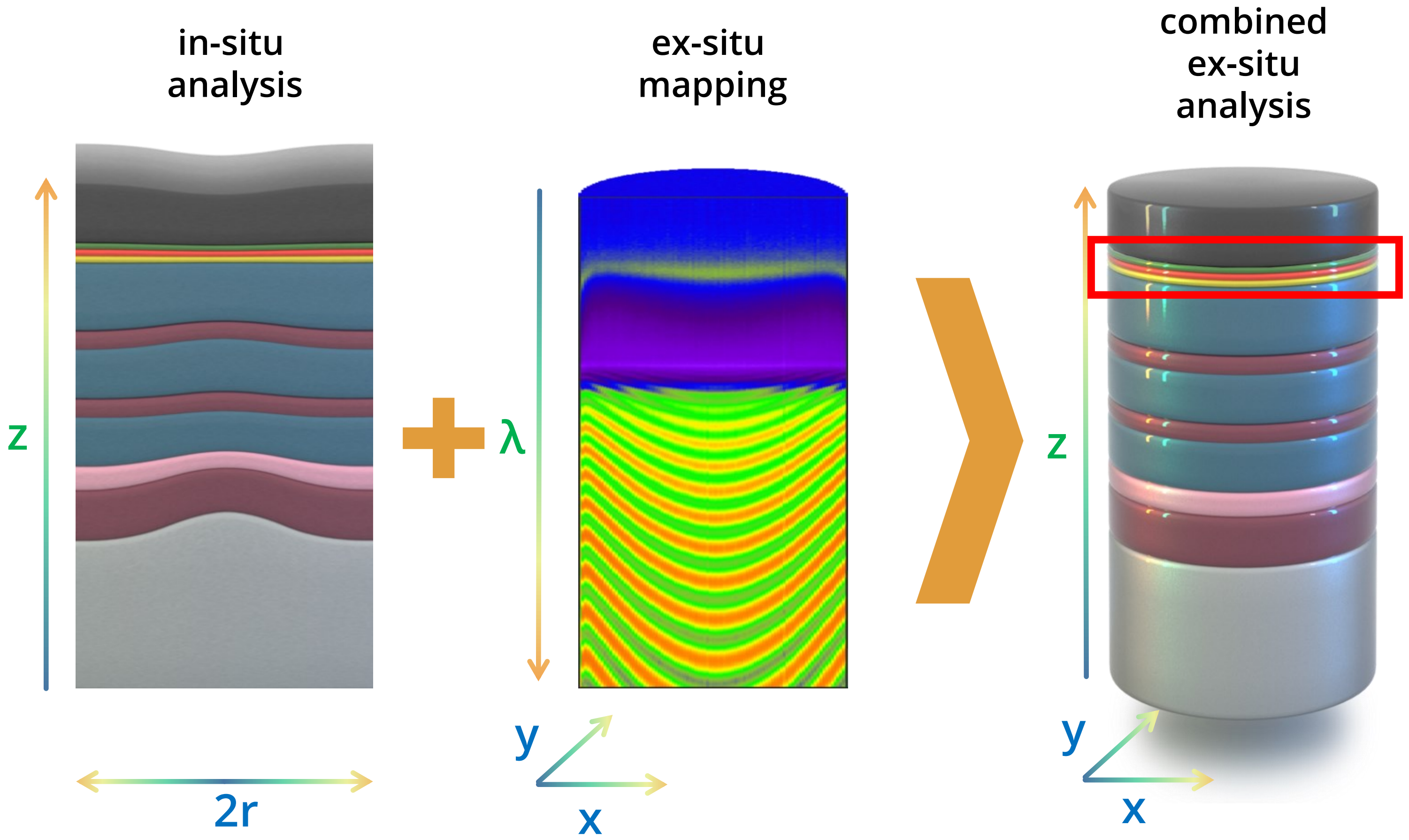




Simulation of E-Mode HEMT with 50 nm p-GaN, spectral fitting of barrier composition & thickness

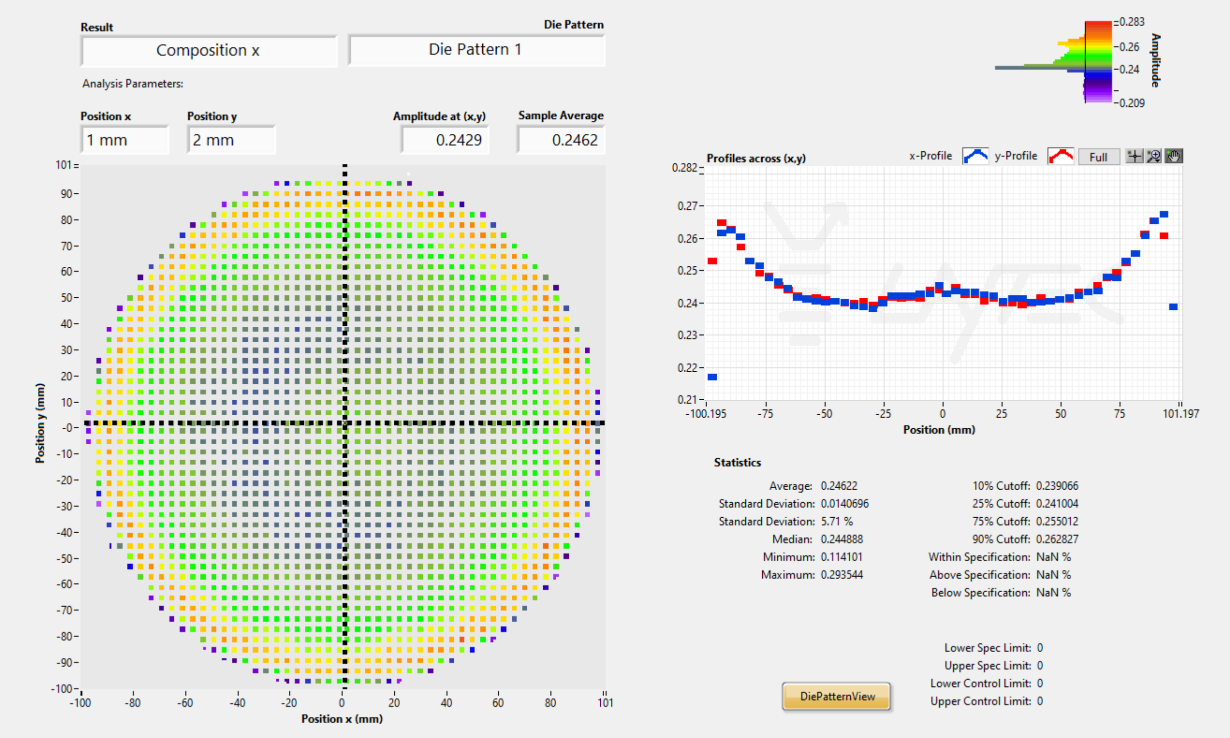


Summary WLR Mapping



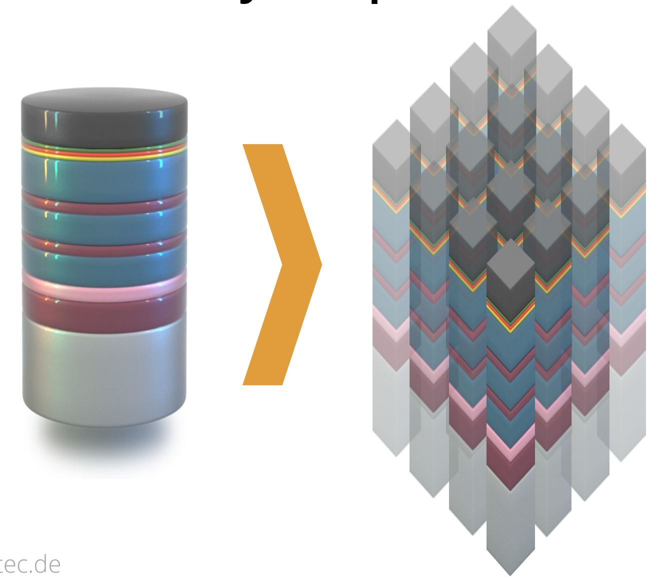
- radial profile of layer properties of entire stack available from in-situ data
- for selected critical layers with suitable spectral signatures:
  - obtain quantification (thickness & composition) resolved in x/y

Step 3 - utilizing one of EpiX's advanced software features: virtual die patterns



Result data: barrier composition – die-level view

- define and apply custom die patterns
- obtain resulting analysis information on die-level
- obtain yield-classification on die-level
- rotate or modify die pattern to improve yield



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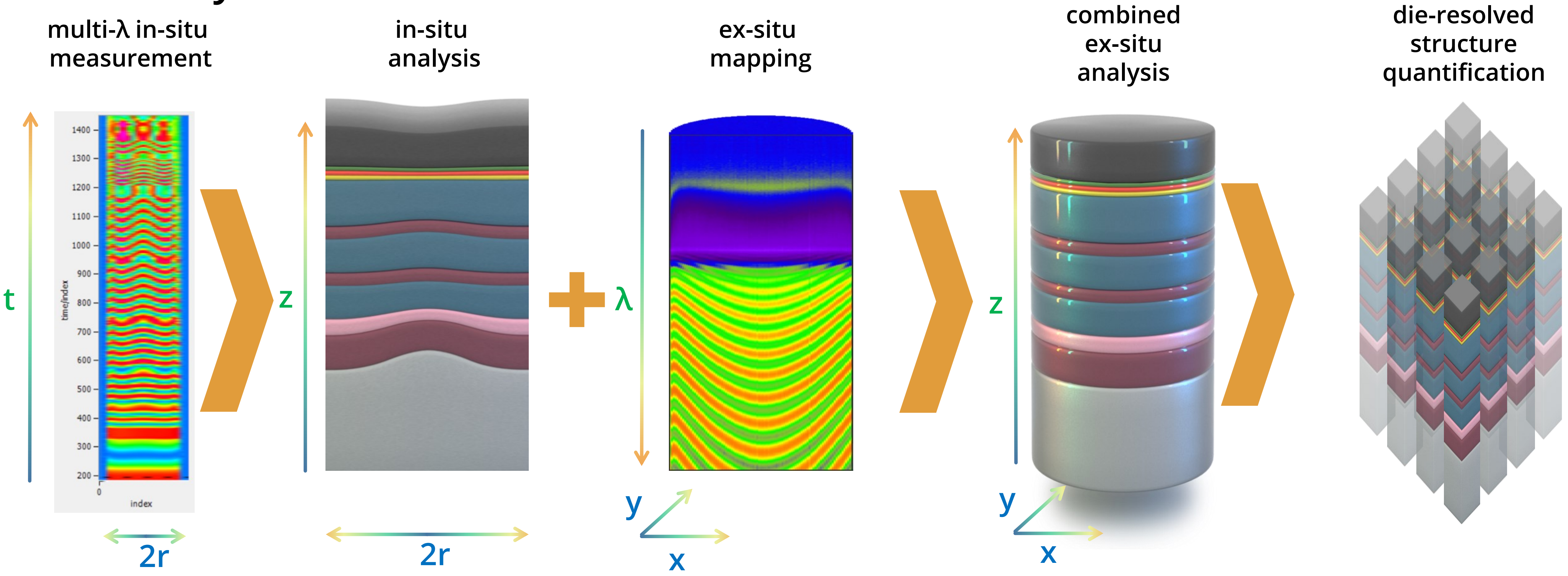
Summary



- By connecting in-situ and ex-situ metrology, we can determine the critical layer parameters of increasingly complex layer structures at die-level
- method presented here for GaN-on-Si examples also valid for many other device types (VCSELS, μLEDs)

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Knowledge is key

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