

ICP Etching Process Improvement by in-situ metrology

Tom Thieme

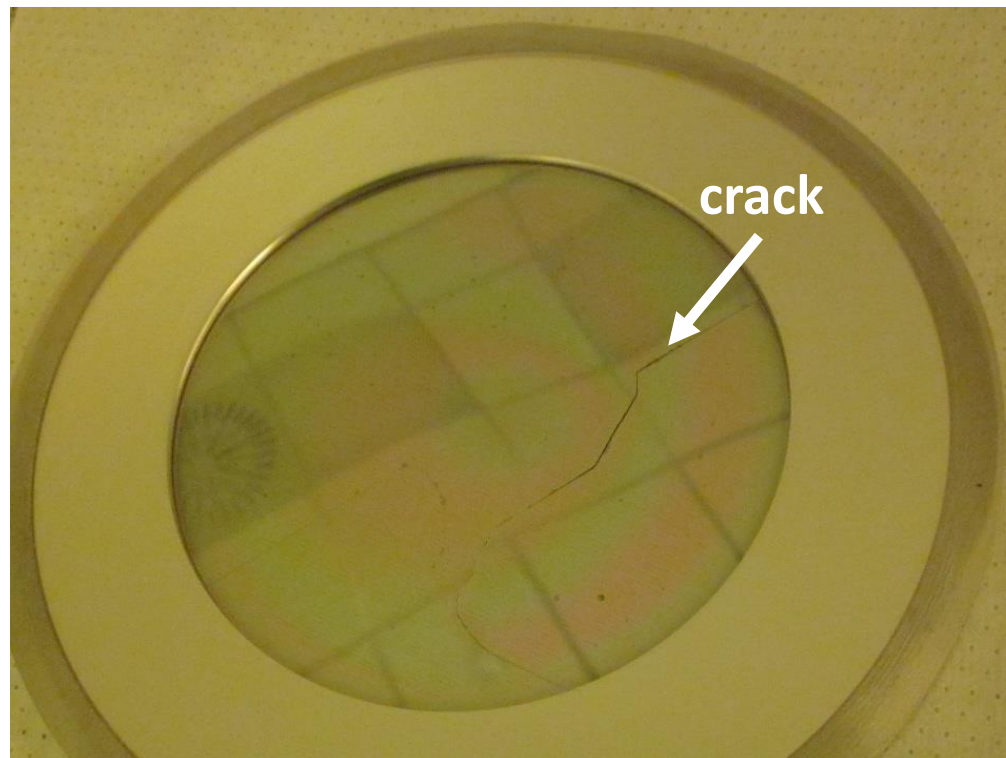
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Issue of cracking wafers (3" and 4"):



Non optimized ICP process results in SiC/GaN wafer cracking due to vertical strain in the carrier/bonding-layer/SiC/GaN structure

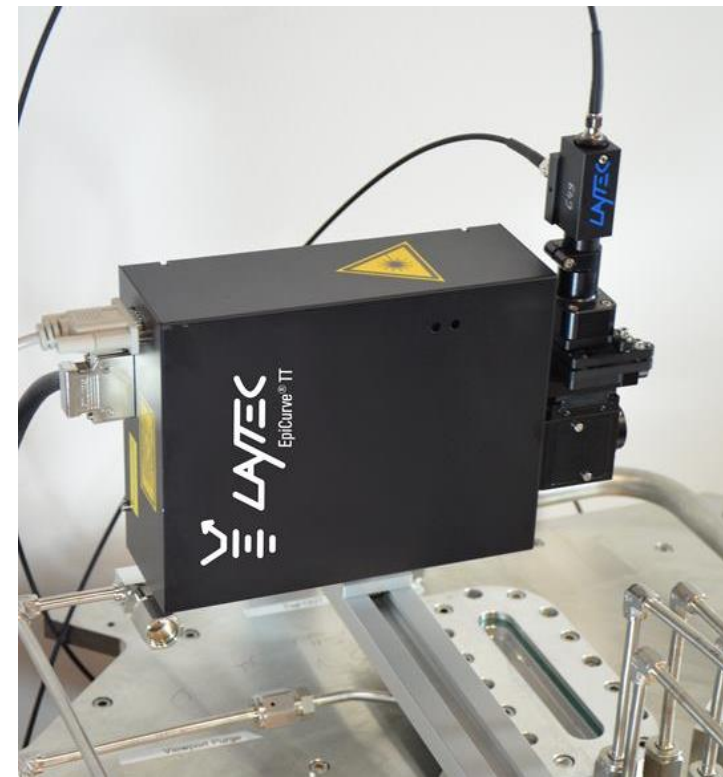
Equipment configuration

- Sentech ICP etching system
 - etch bias strongly depends on carrier
 - etch rate strongly depends on carrier
 - Platen temperature 100... 150 °C
backside cooling, $p = 1000 \text{ Pa}$

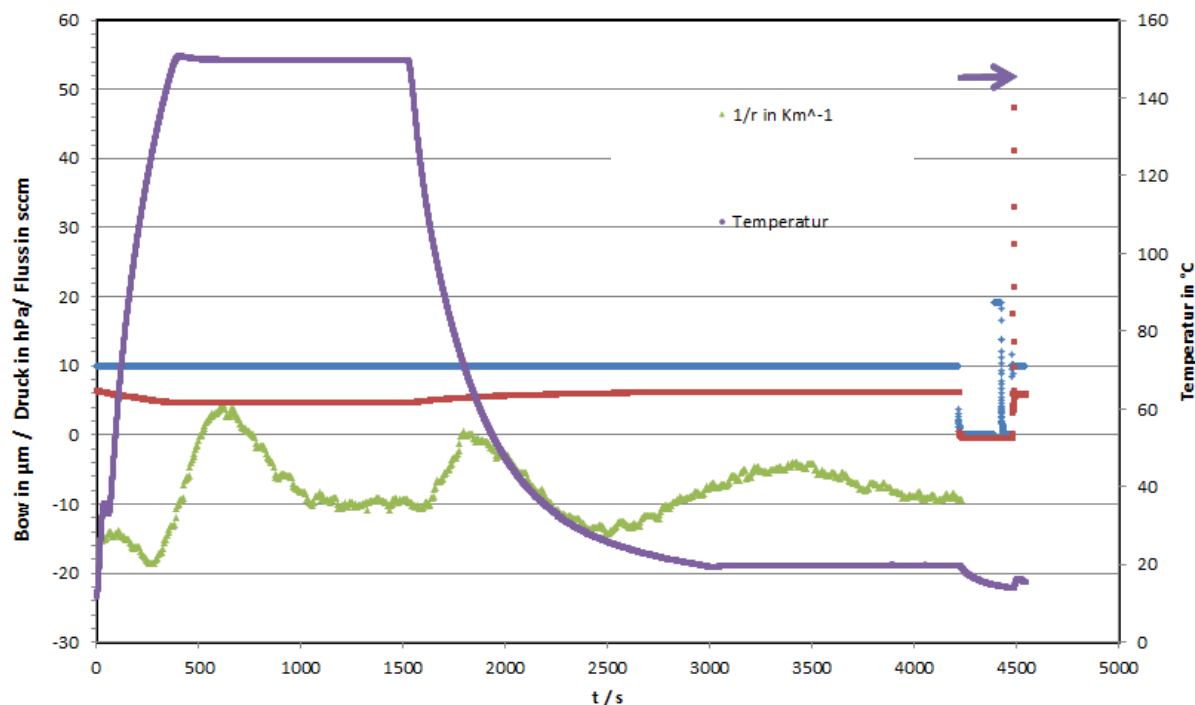


Sentech web side: ICP-RIE plasma etcher SI 500

LayTec EpiCurve system
attached to the view-port:

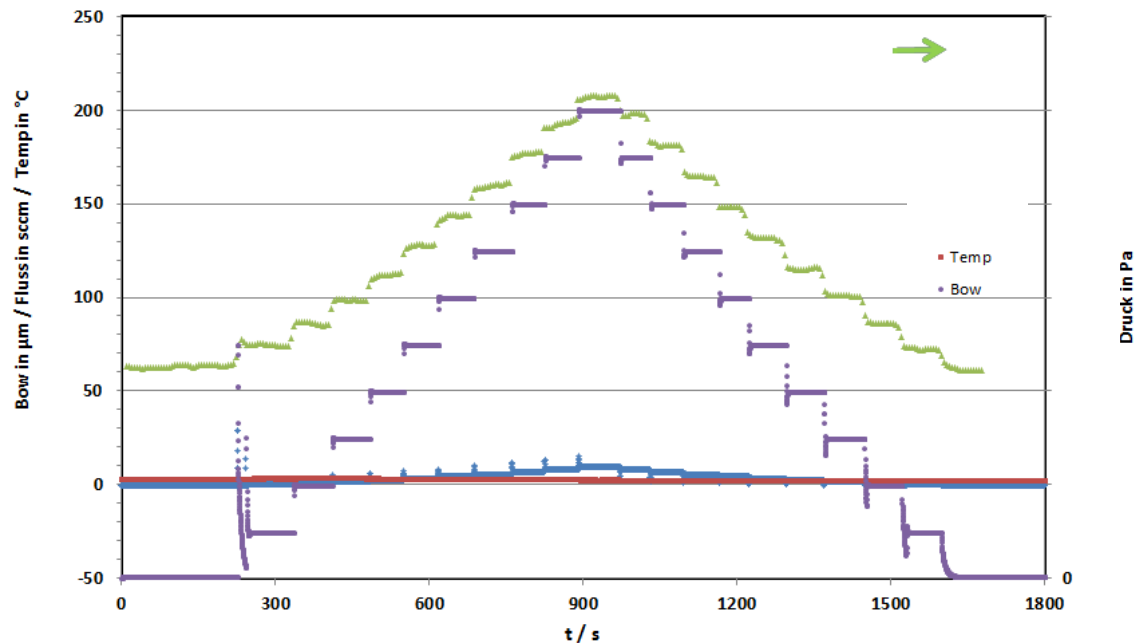


Stress evolution during constant etching conditions



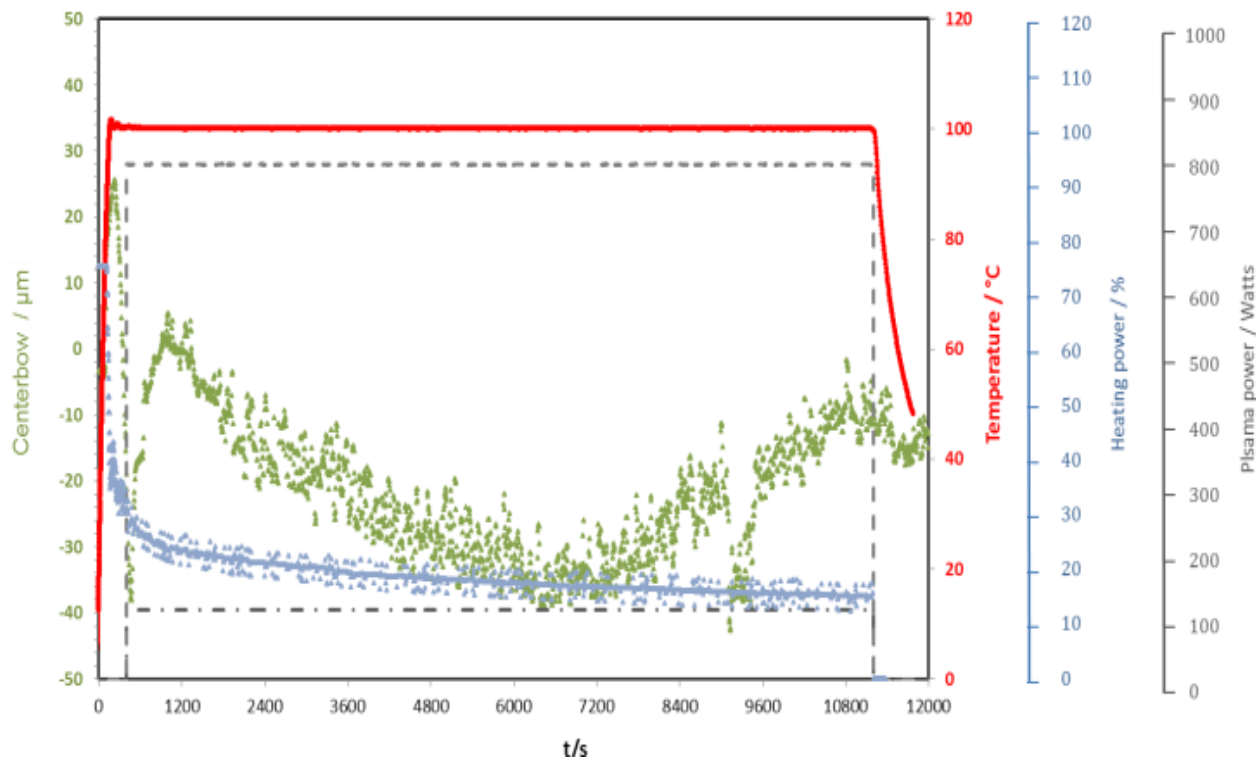
During constant etching conditions stress is incorporated due to temperature gradient of wafer

Stress evolution during various etching conditions



During constant temperature stress is incorporated due to varying etching conditions

Optimized etching process using in-situ products



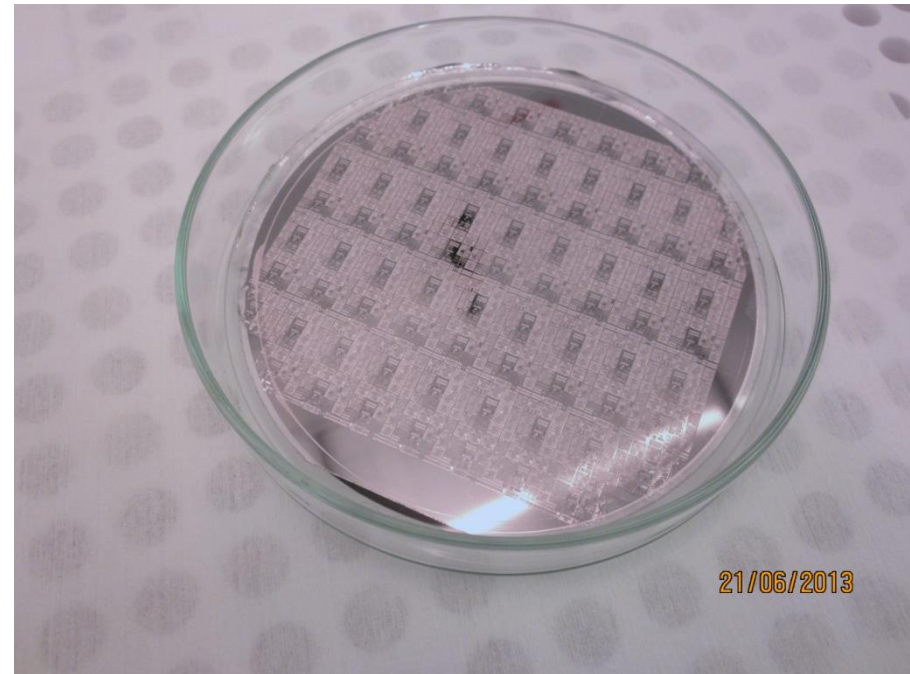
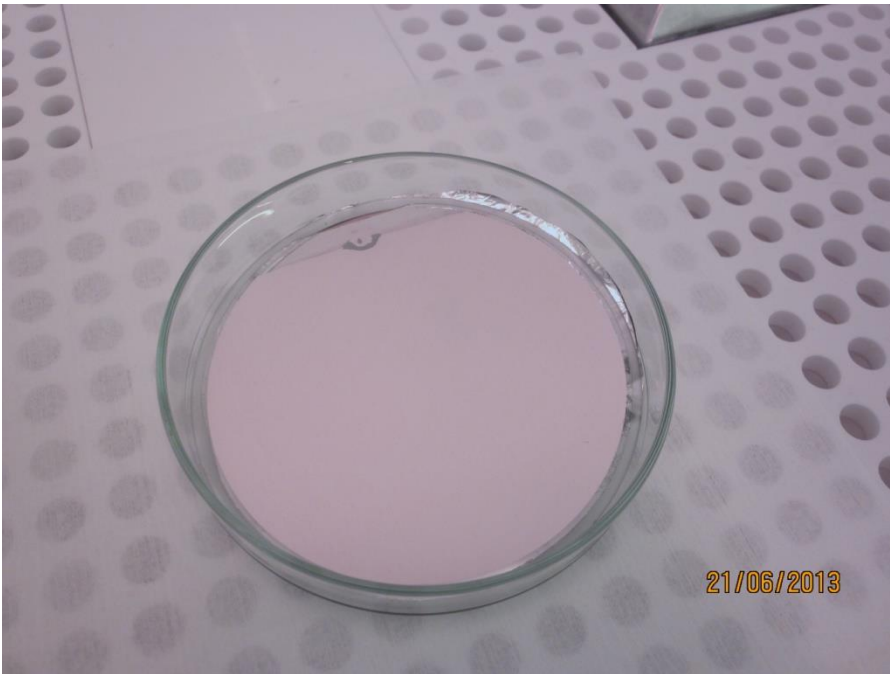
Using curvature measurement, etching process could be optimized

No wafer damage anymore = safe time and cost!

Optimized etching process using in-situ products

Backside

Frontside



(black marks are artefacts due to photography and depend on angle of the shot)

Knowledge is key



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