

LayTec in-situ power for RF and power electronics

GaN/Si, GaN/SiC and SiC/SiC based devices and related MOCVD processes currently gain increasing interest due to the expected growth rates of the power electronics markets. Following this trend, LayTec has further customized its in-situ metrology products for these processes and materials. Our tools help to

fully exploit the intrinsic advantages offered by wide-band-gap materials and to manufacture competitive devices with high-yield and cost-efficient processes. This newsletter gives two examples. Find more results and physical background at www.laytec.de/power-rf-electronics.

EpiNet: expanded nk database and advanced analysis for GaN/SiC-4H HEMTs

AlGaN/GaN and InAlN/GaN device structures are excellent platforms for the production of next generation RF and power electronics (e.g. HEMTs). However, the MOCVD growth of the AlGaN and AlInGaN structures on large SiC-4H wafers needs complex growth recipes for strain management and tight statistical process control (SPC) to obtain high process yields. For this technology, LayTec has expanded its high-temperature nk database and implemented additional real-time analysis routines to feed SPC systems with highly accurate in-situ data.

Fig. 1 gives an example. The initial AlN layer is grown on SiC-4H in a three-step high-temperature process. The 405 nm reflectance is performed at very high wafer temperature (measured by Pyro 400 with ± 0.5 K accuracy) in a sophisticated three-temperature process. This ensures significant defect reduction for the subsequent HEMT growth. Despite the varying wafer temperature in this AlN buffer growth process, the latest real-time analysis function of EpiNet library allows our

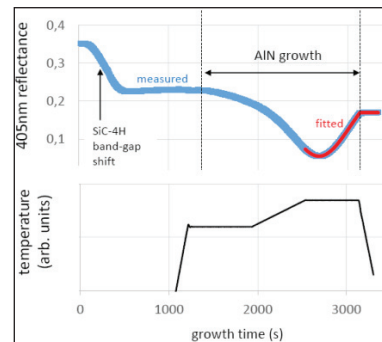


Fig 1: AlN buffer growth on SiC-4H in a three-step high-temperature process. The 405 nm reflectance data is highly accurate due to auto-calibration to the true SiC-4H substrate temperature (blue - measured, red - fitted reflectance). The fit gives $d_{\text{AlN}} = 73.2 \pm 0.5$ nm. Data provided by confidential customer.

tools to reach ± 0.5 nm accuracy in real-time AlN film thickness measurement. This has been achieved by tightly correlating the absolute SiC-4H wafer temperature with high accuracy SiC-4H and AlN nk optical data and implementing new analysis algorithms that separate reflectance changes caused by temperature ramping from the AlN growth effects. For further information please ask info@laytec.de.

Mitsubishi Electric Corp. uses in-situ monitoring for crack-free GaN-on-Si HEMTs

Mitsubishi Electric Corporation reported recently about growth of crack-free low-bowing GaN-on-Si HEMTs [1]. To improve the breakdown voltage and power-added efficiency, Mr. Atsushi Era and his team grow the GaN buffer layer doped with Fe (GaN:Fe). Fig. 2 shows reflectance and curvature measurements during the growth of wafers A and B. The reflectance of A has a clear slump during the GaN:Fe growth, which indicates a rough surface of the GaN:Fe layer. The compressive stress during the GaN growth of A is obviously insufficient to compensate the tensile stress during cooling down. The result is cracking over the whole area of Wafer A.

To suppress 3D island growth in the GaN:Fe, Wafer B is grown with a 100 nm thick undoped GaN interlayer (u-GaN IL) prior to GaN:Fe growth (Fig. 3). The reflectance of B shows no slump, which indicates that the GaN:Fe layer grows nicely in the 2D mode. The compressive stress is well balanced, so that Wafer B is nearly flat after cooling-down. Its smooth, crack-free surface is confirmed by atomic force microscopy (AFM). Furthermore, the electron transfer characteristics of a device fabricated on Wafer B shows an ideal pinch-off behavior. You can find a more detailed report of this study at www.laytec.de/power-rf-electronics.

[1] A. Era *et al.* Growth of crack-free GaN on Si HEMTs with Fe-doped GaN using un-doped GaN interlayer, *ICSCRM proceedings (2015)*

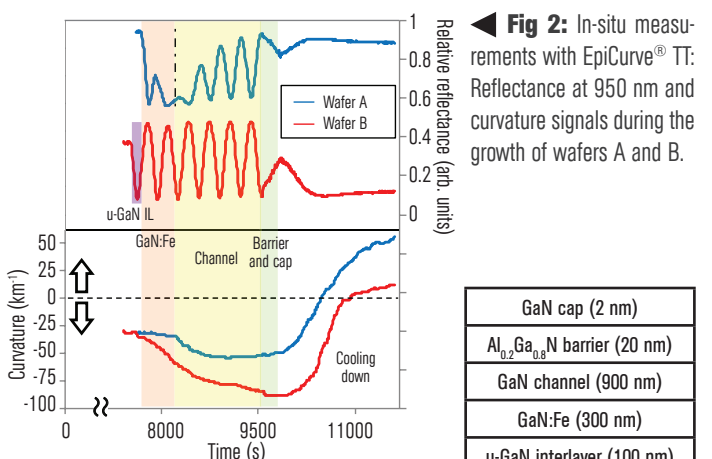


Fig 2: In-situ measurements with EpiCurve® TT: Reflectance at 950 nm and curvature signals during the growth of wafers A and B.

GaN cap (2 nm)
Al _{0.2} Ga _{0.8} N barrier (20 nm)
GaN channel (900 nm)
GaN:Fe (300 nm)
u-GaN interlayer (100 nm)
AlGaN transition layer
AlN nucleation layer
4-inch Si(111) substrate

Fig 3: Layer stack description of Wafer B

You can meet us at the following workshops, conferences and trade fairs:

10–11 December 2015 | **DGKK (Conference of the German Crystal Growth Society)** | Göttingen, Germany | Booth 8

13–18 February 2016 | **SPIE Photonics West 2016** | San Francisco, CA, USA | Talk: "Process control of MOCVD growth for LEDs and other devices"