EpiCurve®: ICP-Etching in a Sentech SI 500 tool

Researchers at Ferdinand-Braun-Institute in Berlin successfully applied EpiCurve® in-situ metrology for optimizing etching recipies in an ICP-RIE plasma etching tool (SI 500, Sentech). With standard etching recipes the SiC/GaN wafer (pasted to a glass or sapphire carrier) frequently cracks because it suffers from a ±50µm wafer bow due to vertical temperature gradients and differences in the thermal expansion coefficients of carrier, substrate and GaN. By means of EpiCurve® in-situ strain engineering the wafer bow was kept down to ±20µm (see Fig.1) and wafer cracking can be completely avoided. For further information please download the presentation of ICP-Etch plasma or visit www.laytec.de/epicurve.

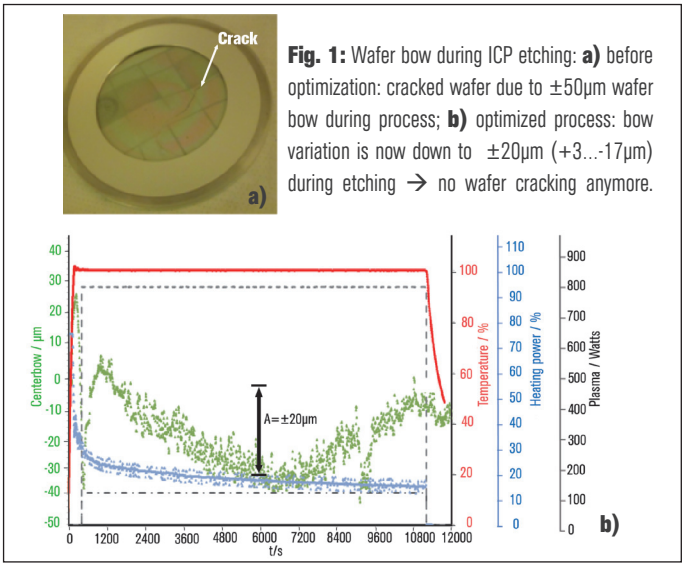

Fig. 1: Wafer bow during ICP etching: **a)** before optimization: cracked wafer due to ±50µm wafer bow during process; **b)** optimized process: bow variation is now down to ±20µm (+3...-17µm) during etching → no wafer cracking anymore.

EpiCurve® TT: Optimization of Evatec's plasma assisted evaporation

Dr. Silvia Schwyn Thöny of Evatec presented in her recent presentation at FOC 2014 latest results on strain engineering for optimized plasma assisted evaporation of SiO_2 and TiO_2 multi-layer structures. First, by separate variation of deposition rate, gas flow and plasma power the related film stress has been determined (Fig.2). Secondly, the deposition recipes have been optimized for minimum total stress in the SiO_2/TiO_2 multi-layer structures. For further information please download the presentation of Evatec or visit www.laytec.de/epicurve.

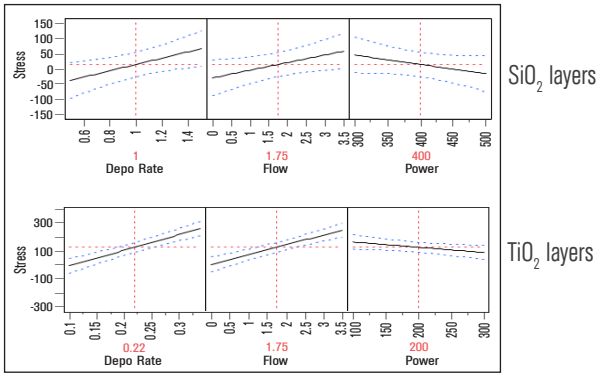

Fig. 2: (Please see text for exlanation!)

EpiTT: Monitoring of SiO_2/SiN_x deposition in a Oxford Instruments ICP CVD tool

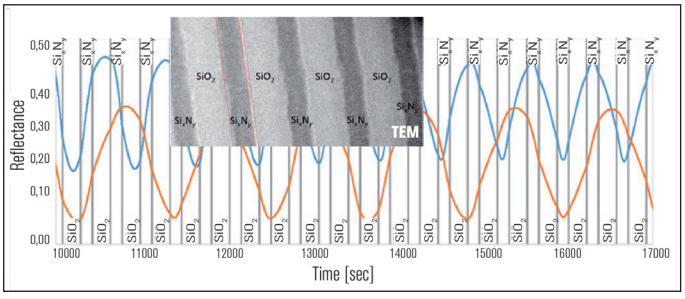

Fig. 3: In-situ data as taken during growth of a multi-layer stack (50 layer pairs; target thicknesses: 400 Å of SiO_2 and 180 Å of SiN_x). The details of the two-wavelength reflectance transients (405nm: blue line and 633nm: orange line) depend on the specific growth rates and deposition conditions.

In a collaboration between LayTec and University of Ilmenau (Germany) it was demonstrated that an EpiTT with optimized hardware and software (EpiTT 3DStaR) can analyze quantitatively nano-scaled SiO_2/SiN_x multilayer stacks (see Fig.3). The thicknesses determined by in-situ are fully consistent to transmission electron microscopy (TEM) images. For further information please download the application note EpiTT 3DStaR or visit www.laytec.de/epitt.

You can meet us at the following workshops, conferences and trade fairs:

4 – 6 Feb 2015 | LED Korea 2015 | Seoul, Korea | Volker Blank (LayTec) presents: Real-time MOCVD Process Control of Wafer Temperature, Growth Rate and Wafer Bow for High Performance III-Nitride Devices | www.led-korea.org/en/

7 – 12 Feb 2015 | SPIE 2015 | San Francisco, CA, USA | Dr. Stephanie Fritze (LayTec) presents: In-situ metrology–key enabling technology for LED and LD production & GaN on Si: new approaches for stress engineering and doping | www.spie.org

11 – 12 March 2015 | CS INTERNATIONAL 2015 | Frankfurt, Germany | Dr. Kolja Haberland (CTO, LayTec) presents: Advanced in-situ metrology for III-V on silicon technology | www.cs-international.net